PCM1795 32-Bit, 192-kHz Sampling, Advanced Segment, Stereo Audio Digital-to-Analog Converter

1 Features

- 32-Bit Resolution
- Analog Performance:
  - Dynamic Range: 123 dB
  - THD+N: 0.0005%
- Differential Current Output: 3.9 mA_{PP}
- 8× Oversampling Digital Filter:
  - Stop-Band Attenuation: –98 dB
  - Passband Ripple: ±0.0002 dB
- Sampling Frequency: 10 kHz to 200 kHz
- System Clock: 128, 192, 256, 384, 512, or 768 f_S With Autodetect
- Accepts 16-, 24-, and 32-Bit Audio Data
- PCM Data Formats: Standard, I^2S, and Left-Justified
- DSD Format Interface Available
- Interface Available for Optional External Digital Filter or DSP
- TDMCA or Serial Port (SPI™/I^2C)
- User-Programmable Mode Controls:
  - Digital Attenuation: 0 dB to –120 dB, 0.5-dB/Step
  - Digital De-Emphasis
  - Digital Filter Roll-Off: Sharp or Slow
  - Soft Mute
  - Zero Flag for Each Output
- Compatible With PCM1792A and PCM1796 (Pins and Mode Controls)
- Dual Supply Operation:
  - 5-V Analog, 3.3-V Digital
- 5-V Tolerant Digital Inputs
- Small SSOP-28 Package

2 Applications

- A/V Receivers
- SACD Players
- DVD Players
- HDTV Receivers
- Car Audio Systems
- Digital Multitrack Recorders
- Other Applications Requiring 32-Bit Audio

3 Description

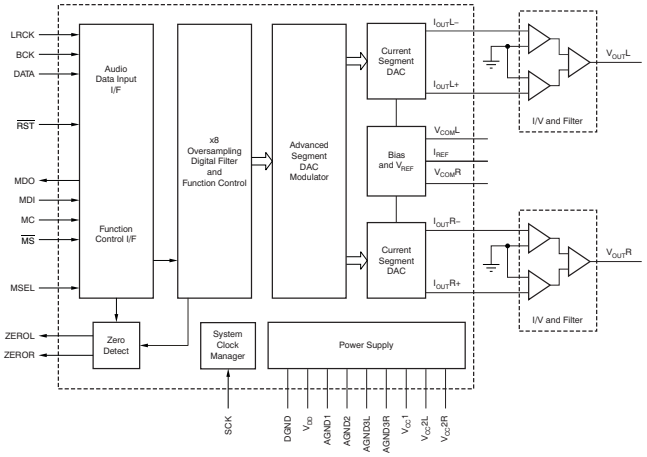
The PCM1795 device is a monolithic CMOS integrated circuit that includes stereo digital-to-analog converters (DACs) and support circuitry in a small SSOP-28 package. The data converters use TI's advanced segment DAC architecture to achieve excellent dynamic performance and improved tolerance to clock jitter. The PCM1795 provides balanced current outputs, letting the user optimize analog performance externally. The PCM1795 accepts pulse code modulation (PCM) and direct stream digital (DSD) audio data formats, thus providing an easy interface to audio digital signal processors (DSPs) and decoder chips. The PCM1795 device also interfaces with external digital filter devices such as the DF1704, DF1706, and the PMD200 from Pacific Microsonics™. Sampling rates up to 200 kHz are supported. A full set of user-programmable functions is accessible through an SPI or I^2C serial control port that supports register write and readback functions. The PCM1795 device also supports the time-division-multiplexed (TDM) command and audio (TDMCA) data format.

Device Information[1]

PART NUMBER	PACKAGE	BODY SIZE (NOM)
PCM1795	SSOP (28)	10.20 mm × 5.30 mm

(1) For all available packages, see the orderable addendum at the end of the data sheet.

Block Diagram



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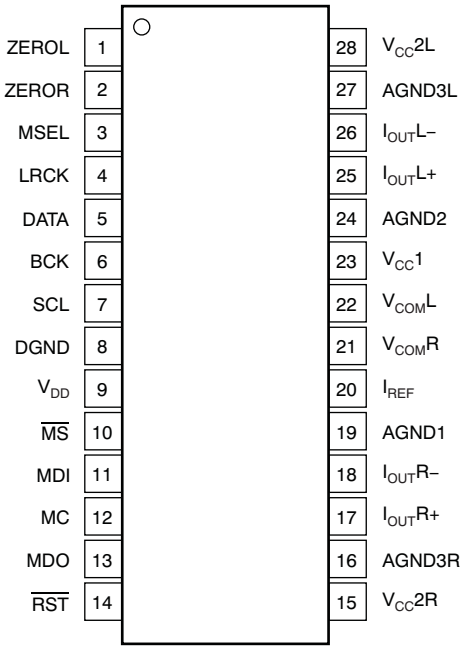
4 Revision History

Changes from Original (May 2009) to Revision A **Page**

- Added *Pin Configuration and Functions* section, *ESD Rating* table, *Recommended Operating Conditions* table, *Feature Description* section, *Device Functional Modes*, *Application and Implementation* section, *Power Supply Recommendations* section, *Layout* section, *Device and Documentation Support* section, and *Mechanical, Packaging, and Orderable Information* section ... 1

5 Pin Configuration and Functions

DB Package
28-Pin SSOP
(Top View)



Pin Functions

PIN		TYPE	DESCRIPTION
NAME	NO.		
AGND1	19	—	Analog ground (internal bias)
AGND2	24	—	Analog ground (internal bias)
AGND3L	27	—	Analog ground (left channel DACFF)
AGND3R	16	—	Analog ground (right channel DACFF)
BCK	6	Input	Bit clock input(1)
DATA	5	Input	Serial audio data input(1)
DGND	8	—	Digital ground
$I_{OUT}L+$	25	Output	Left channel analog current output+
$I_{OUT}L–$	26	Output	Left channel analog current output–
$I_{OUT}R+$	17	Output	Right channel analog current output+
$I_{OUT}R–$	18	Output	Right channel analog current output–
I_{REF}	20	—	Output current reference bias pin
LRCK	4	Input	Left and right clock (f_S) input(1)
MC	12	Input	Mode control clock input(1)
MDI	11	Input	Mode control data input(1)
MDO	13	Input or Output	Mode control read-back data output(2)
$\overline{MS}$	10	Input or Output	Mode control chip-select input(3); active low
MSEL	3	Input	$I^2C/\overline{SPI}$ select(1); active low SPI select

(1) Schmitt-trigger input, 5-V tolerant.
(2) Schmitt-trigger input and output. 5-V tolerant input. In I^2C mode, this pin becomes an open-drain 3-state output; otherwise, this pin is a CMOS output.
(3) Schmitt-trigger input and output. 5-V tolerant input and CMOS output.

Pin Functions (continued)

PIN		TYPE	DESCRIPTION
NAME	NO.		
$\overline{RST}$	14	Input	Reset(1); active low
SCK	7	Input	System clock input(1)
$V_{CC}1$	23	—	Analog power supply, 5 V
$V_{CC}2L$	28	—	Analog power supply (left channel DACFF), 5 V
$V_{CC}2R$	15	—	Analog power supply (right channel DACFF), 5 V
$V_{COM}L$	22	—	Left channel internal bias decoupling pin
$V_{COM}R$	21	—	Right channel internal bias decoupling pin
V_{DD}	9	—	Digital power supply, 3.3 V
ZEROL	1	Input or Output	Zero flag for left channel(3)
ZEROR	2	Input or Output	Zero flag for right channel(3)

6 Specifications

6.1 Absolute Maximum Ratings(1)

Over operating free-air temperature range, unless otherwise noted.

		MIN	MAX	UNIT
Supply voltage	$V_{CC}1$, $V_{CC}2L$, $V_{CC}2R$	–0.3	6.5	V
	V_{DD}	–0.3	4	V
Supply voltage differences	$V_{CC}1$, $V_{CC}2L$, $V_{CC}2R$	–0.1	0.1	V
Ground voltage differences	AGND1, AGND2, AGND3L, AGND3R, DGND	–0.1	0.1	V
Digital input voltage	LRCK, DATA, BCK, SCK, MSEL, $\overline{RST}$, $\overline{MS}$ (2), MDI, MC, MDO(2), ZEROL(2), ZEROR(2)	–0.3	6.5	V
	ZEROL(3), ZEROR(3), MDO(3), $\overline{MS}$ (3)	–0.3	(V_{DD} + 0.3) < 4	V
Analog input voltage		–0.3	(V_{CC} + 0.3) < 6.5	V
Input current (any pins except supplies)		–10	10	mA
Ambient temperature under bias		–40	125	°C
Junction temperature			150	°C
Package temperature (IR reflow, peak)			260	°C
Storage temperature, T_{stg}		–55	150	°C

(1) Stresses beyond those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under *Recommended Operating Conditions* is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
(2) Input mode or I^2C mode.
(3) Output mode except for I^2C mode.

6.2 ESD Ratings

			VALUE	UNIT
$V_{(ESD)}$	Electrostatic discharge	Human body model (HBM), per ANSI/ESDA/JEDEC JS-001(1)	±3000	V
		Charged-device model (CDM), per JEDEC specification JESD22-C101(2)	±1500	

(1) JEDEC document JEP155 states that 500-V HBM allows safe manufacturing with a standard ESD control process.
(2) JEDEC document JEP157 states that 250-V CDM allows safe manufacturing with a standard ESD control process.

6.3 Recommended Operating Conditions

over operating free-air temperature range (unless otherwise noted)

		MIN	NOM	MAX	UNIT
VDD Digital supply voltage		3.0	3.3	3.6	V
VCC1	Analog Supply Voltage	4.7525	5	5.25	V
VCC2L					
VCC2R					
Operating Temperature		–25		85	°C

6.4 Thermal Information

THERMAL METRIC[1]		PCM1795 DB (SSOP) 28 PINS	UNIT
$R_{\theta JA}$	Junction-to-ambient thermal resistance	70.3	°C/W
$R_{\theta JC(top)}$	Junction-to-case (top) thermal resistance	28.3	
$R_{\theta JB}$	Junction-to-board thermal resistance	31.5	
ψ_{JT}	Junction-to-top characterization parameter	2.9	
ψ_{JB}	Junction-to-board characterization parameter	31.1	
$R_{\theta JC(bot)}$	Junction-to-case (bottom) thermal resistance	—	

(1) For more information about traditional and new thermal metrics, see the *IC Package Thermal Metrics* application report (SPRA953).

6.5 Electrical Characteristics

All specifications at T_A = +25°C, $V_{CC}1 = V_{CC}2L = V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, system clock = 256 f_S, and 32-bit data, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
RESOLUTION						
	Resolution			32		Bits
DATA FORMAT (PCM Mode)						
	Audio data interface format			Standard, I^2S, left-justified		
	Audio data bit length			16-, 24-, 32-bit selectable		
	Audio data format			MSB first, twos complement		
f_S	Sampling frequency		10		200	kHz
	System clock frequency			128, 192, 256, 384, 512, 768		f_S
DATA FORMAT (DSD Mode)						
	Audio data interface format			DSD (direct stream digital)		
	Audio data bit length			1		Bit
f_S	Sampling frequency			2.8224		MHz
	System clock frequency		2.8224		11.2986	MHz
DIGITAL INPUT/OUTPUT						
	Logic family			TTL compatible		
V_{IH}	Input logic level		2			VDC
V_{IL}					0.8	VDC
I_{IH}	Input logic current	$V_{IN} = V_{DD}$			10	µA
I_{IL}		V_{IN} = 0 V			–10	µA
V_{OH}	Output logic level	I_{OH} = –2 mA	2.4			VDC
V_{OL}		I_{OL} = 2 mA			0.4	VDC
DYNAMIC PERFORMANCE (PCM MODE)[1][2]						
THD+N at V_{OUT} = 0 dB		f_S = 48 kHz		0.0005%	0.001%	
		f_S = 96 kHz		0.001%		
		f_S = 192 kHz		0.0015%		
Dynamic range		EIAJ, A-weighted, f_S = 48 kHz	120	123		dB
		EIAJ, A-weighted, f_S = 96 kHz		123		
		EIAJ, A-weighted, f_S = 192 kHz		123		

(1) Filter condition:
THD+N: 20-Hz high-pass filter (HPF), 20-kHz AES17 low-pass filter (LPF)
Dynamic range: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Signal-to-noise ratio: 20-Hz HPF, 20-kHz AES17 LPF, A-weighted
Channel separation: 20-Hz HPF, 20-kHz AES17 LPF
Analog performance specifications are measured using the System Two™ Cascade audio measurement system by Audio Precision™ in the averaging mode.
(2) Dynamic performance and dc accuracy are specified at the output of the post-amplifier as shown in Figure 53.

Electrical Characteristics (continued)

All specifications at T_A = +25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, system clock = 256 f_S, and 32-bit data, unless otherwise noted.

PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Signal-to-noise ratio	EIAJ, A-weighted, f_S = 48 kHz	120	123		dB
	EIAJ, A-weighted, f_S = 96 kHz		123		
	EIAJ, A-weighted, f_S = 192 kHz		123		
Channel separation	f_S = 48 kHz	116	119		dB
	f_S = 96 kHz		118		
	f_S = 192 kHz		117		
Level linearity error	V_{OUT} = –120 dB		±1		dB
DYNAMIC PERFORMANCE (MONO MODE)(1)(2)(3)					
THD+N at V_{OUT} = 0 dB	f_S = 48 kHz		0.0005%		
	f_S = 96 kHz		0.001%		
	f_S = 192 kHz		0.0015%		
Dynamic range	EIAJ, A-weighted, f_S = 48 kHz		126		dB
	EIAJ, A-weighted, f_S = 96 kHz		126		
	EIAJ, A-weighted, f_S = 192 kHz		126		
Signal-to-noise ratio	EIAJ, A-weighted, f_S = 48 kHz		126		dB
	EIAJ, A-weighted, f_S = 96 kHz		126		
	EIAJ, A-weighted, f_S = 192 kHz		126		
DSD MODE DYNAMIC PERFORMANCE (44.1 kHz, 64 f_S)(1)(4)					
THD+N at FS	2 V rms		0.0007%		
Dynamic range	–60 dB, EIAJ, A-weighted		122		dB
Signal-to-noise ratio	EIAJ, A-weighted		122		dB
ANALOG OUTPUT					
Gain error		–7	±2	7	% of FSR
Gain mismatch, channel-to-channel		–3	±0.5	3	% of FSR
Bipolar zero error	At BPZ	–2	±0.5	2	% of FSR
Output current	Full-scale (0 dB)		4		mA_{PP}
Center current	At BPZ		–3.5		mA
DIGITAL FILTER PERFORMANCE					
De-emphasis error				±0.1	dB

(3) Dynamic performance and dc accuracy are specified at the output of the measurement circuit as shown in Figure 55.
(4) Dynamic performance and dc accuracy are specified at the output of the post-amplifier as shown in Figure 54.

Electrical Characteristics (continued)

All specifications at T_A = +25°C, $V_{CC}1$ = $V_{CC}2L$ = $V_{CC}2R$ = 5 V, V_{DD} = 3.3 V, f_S = 48 kHz, system clock = 256 f_S, and 32-bit data, unless otherwise noted.

PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
FILTER CHARACTERISTICS–1: SHARP ROLL-OFF						
Passband		±0.0002 dB			0.454	f_S
		–3 dB			0.49	
Stop band			0.546			f_S
Passband ripple					±0.0002	dB
Stop-band attenuation		Stop band = 0.546 f_S	–98			dB
Delay time				38/f_S		s
FILTER CHARACTERISTICS–2: SLOW ROLL-OFF						
Passband		±0.001 dB			0.21	f_S
		–3 dB			0.448	
Stop band			0.79			f_S
Passband ripple					±0.001	dB
Stop-band attenuation		Stop band = 0.732 f_S	–80			dB
Delay time				38/f_S		s
POWER-SUPPLY REQUIREMENTS						
V_{DD}	Voltage range		3	3.3	3.6	VDC
$V_{CC}1$			4.75	5	5.25	VDC
$V_{CC}2L$						
$V_{CC}2R$						
I_{DD}	Supply current[5]	f_S = 48 kHz		6	8	mA
		f_S = 96 kHz		11		
		f_S = 192 kHz		21		
I_{CC}		f_S = 44.1 kHz		18	23	
		f_S = 96 kHz		19		
		f_S = 192 kHz		20		
Power dissipation[5]		f_S = 48 kHz		110	141	mW
		f_S = 96 kHz		131		
		f_S = 192 kHz		166		
TEMPERATURE RANGE						
Operating temperature			–25		+85	°C

(5) Input is bipolar zero (BPZ) data.

6.6 Timing Requirements

			MIN	MAX	UNIT
$f_{(SCL)}$	SCL clock frequency	Standard		100	kHz
		Fast		400	
$t_{(BUF)}$	Bus free time between stop and start conditions	Standard	4.7		µs
		Fast	1.3		
$t_{(LOW)}$	Low period of the SCL clock	Standard	4.7		µs
		Fast	1.3		
$t_{(HI)}$	High period of the SCL clock	Standard	4		µs
		Fast	600		ns
$t_{(RS-SU)}$	Setup time for (repeated) start condition	Standard	4.7		µs
		Fast	600		ns
$t_{(S-HD)}$ $t_{(RS-HD)}$	Hold time for (repeated) start condition	Standard	4		µs
		Fast	600		ns
$t_{(D-SU)}$	Data setup time	Standard	250		ns
		Fast	100		
$t_{(D-HD)}$	Data hold time	Standard	0	900	ns
		Fast	0	900	
$t_{(SCL-R)}$	Rise time of SCL signal	Standard	20 + 0.1 C_B	1000	ns
		Fast	20 + 0.1 C_B	300	
$t_{(SCL-R1)}$	Rise time of SCL signal after a repeated start condition and after an acknowledge bit	Standard	20 + 0.1 C_B	1000	ns
		Fast	20 + 0.1 C_B	300	
$t_{(SCL-F)}$	Fall time of SCL signal	Standard	20 + 0.1 C_B	1000	ns
		Fast	20 + 0.1 C_B	300	
$t_{(SDA-R)}$	Rise time of SDA signal	Standard	20 + 0.1 C_B	1000	ns
		Fast	20 + 0.1 C_B	300	
$t_{(SDA-F)}$	Fall time of SDA signal	Standard	20 + 0.1 C_B	1000	ns
		Fast	20 + 0.1 C_B	300	
$t_{(P-SU)}$	Setup time for stop condition	Standard	4		µs
		Fast	600		ns
$C_{(B)}$	Capacitive load for SDA and SCL line			400	pF
$t_{(SP)}$	Pulse duration of suppressed spike	Fast		50	ns
V_{NH}	Noise margin at high level for each connected device (including hysteresis)		0.2 V_{DD}		V

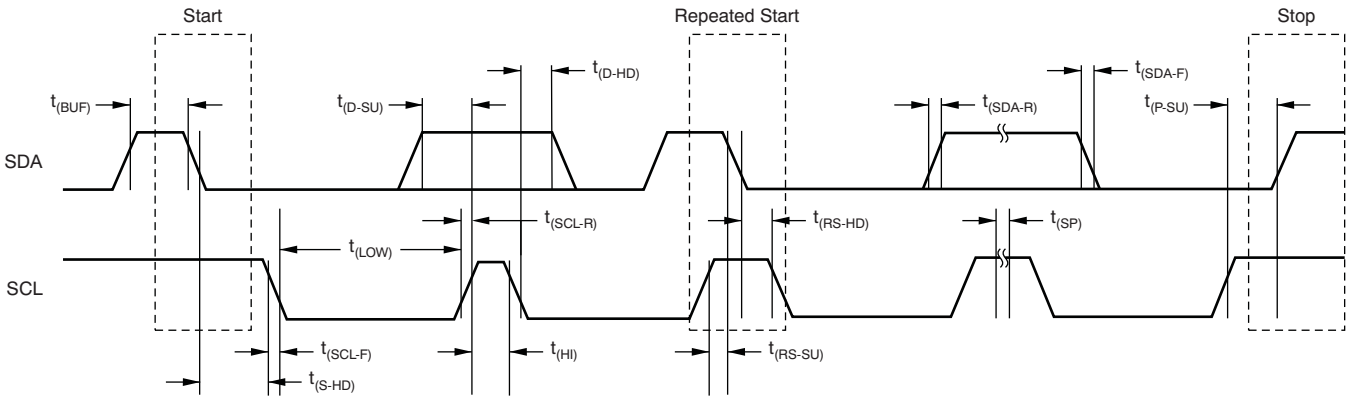


Figure 1. Timing Definition on the I²C Bus

6.7 Typical Characteristics

6.7.1 Digital Filter

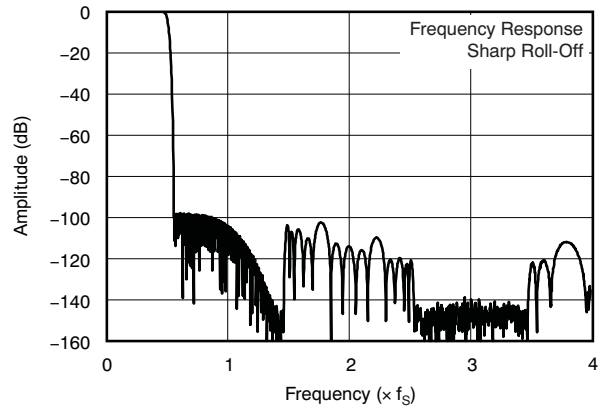


Figure 2. Amplitude vs Frequency

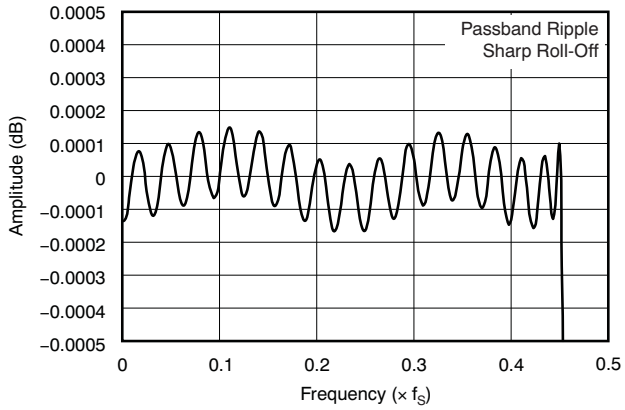


Figure 3. Amplitude vs Frequency

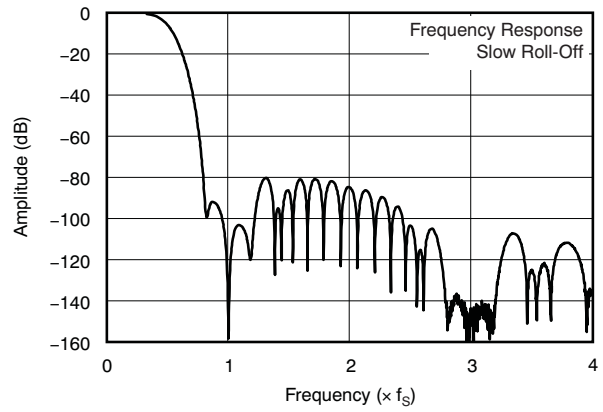


Figure 4. Amplitude vs Frequency

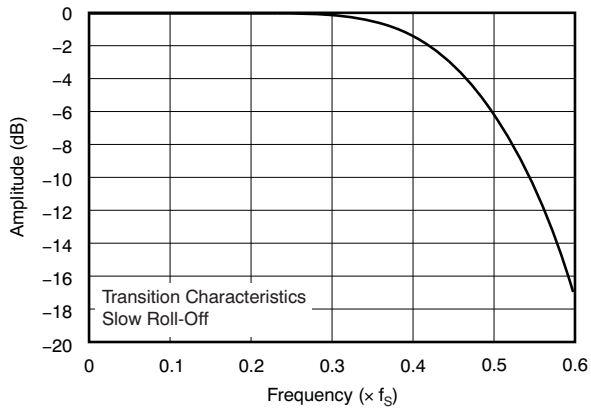


Figure 5. Amplitude vs Frequency

6.7.2 Digital Filter: De-Emphasis Filter

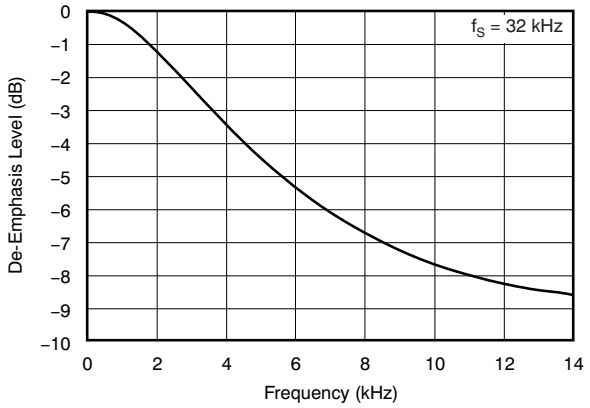


Figure 6. De-Emphasis Level vs Frequency

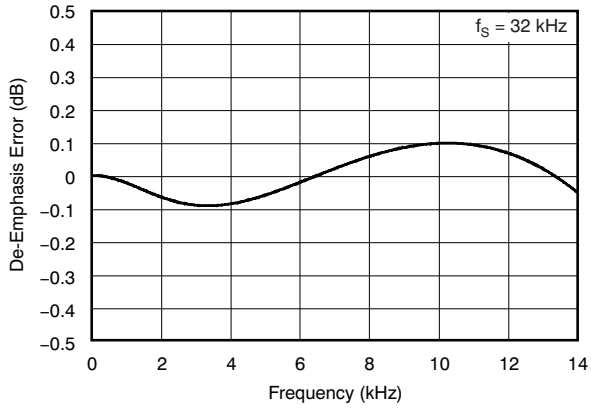


Figure 7. De-Emphasis Error vs Frequency

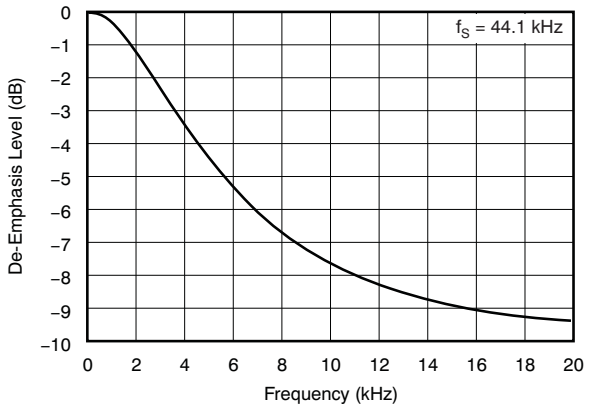


Figure 8. De-Emphasis Level vs Frequency

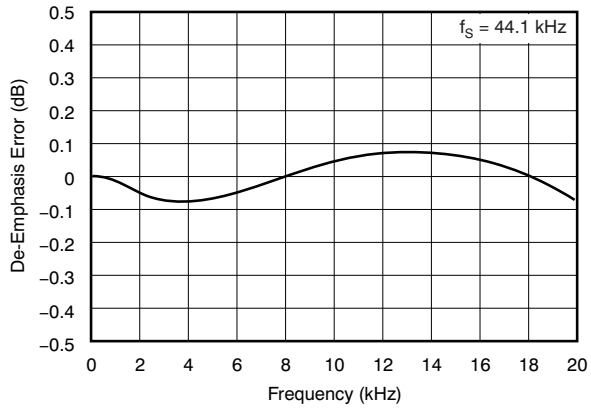


Figure 9. De-Emphasis Error vs Frequency

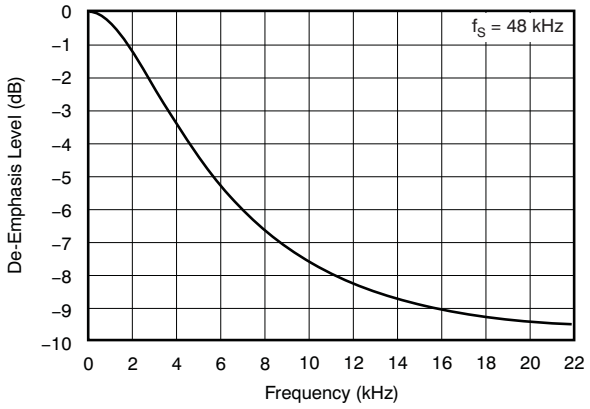


Figure 10. De-Emphasis Level vs Frequency

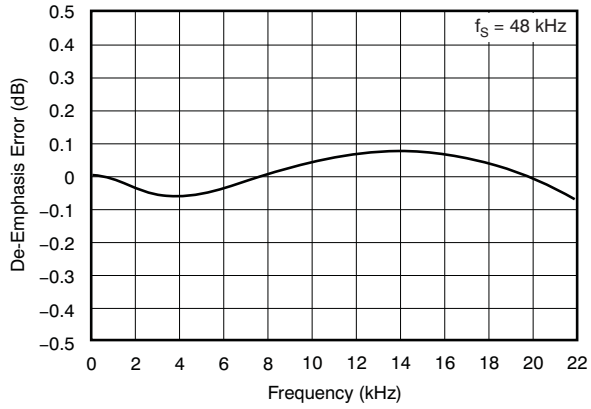


Figure 11. De-Emphasis Error vs Frequency

6.7.3 Analog Dynamic Performance: Supply Voltage Characteristics

PCM mode, T_A = +25°C, and V_{DD} = 3.3 V; measured with circuit shown in Figure 53, unless otherwise noted.

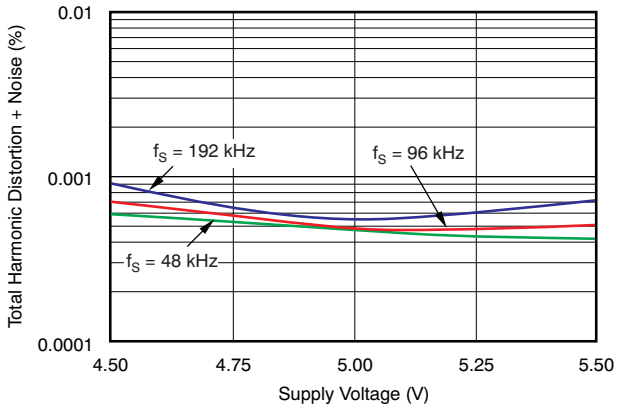


Figure 12. THD+N vs Supply Voltage

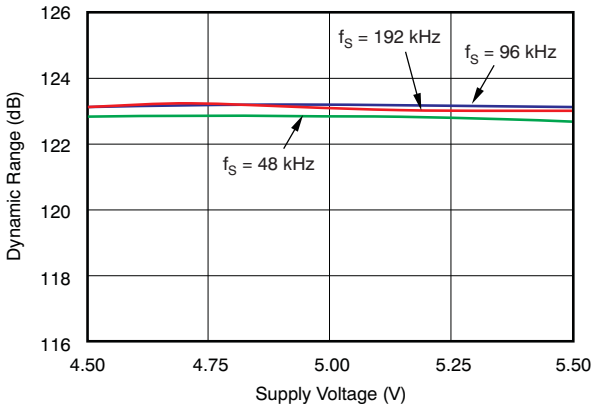


Figure 13. Dynamic Range vs Supply Voltage

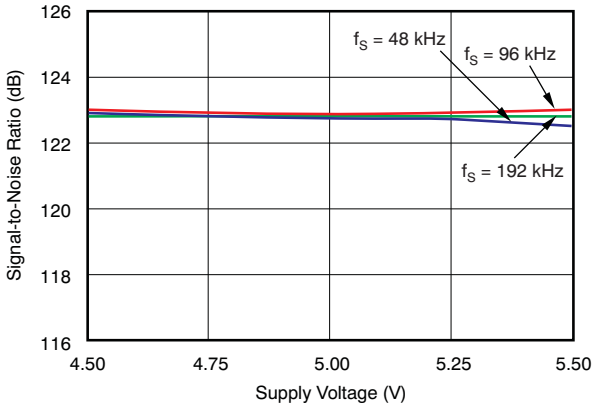


Figure 14. SNR vs Supply Voltage

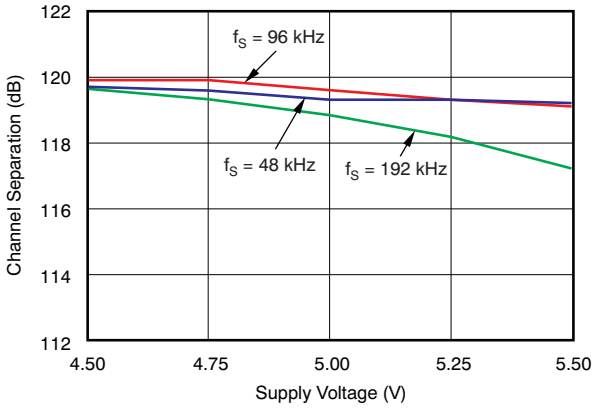


Figure 15. Channel Separation vs Supply Voltage

6.7.4 Analog Dynamic Performance: Temperature Characteristics

PCM mode, V_{DD} = 3.3 V, and V_{CC} = 5 V; measured with circuit shown in Figure 53, unless otherwise noted.

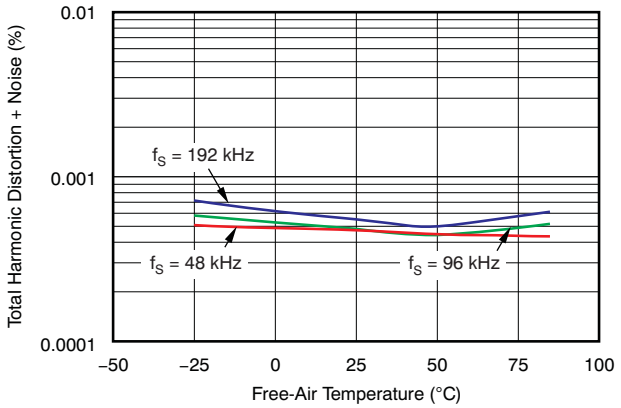


Figure 16. THD+N vs Free-Air Temperature

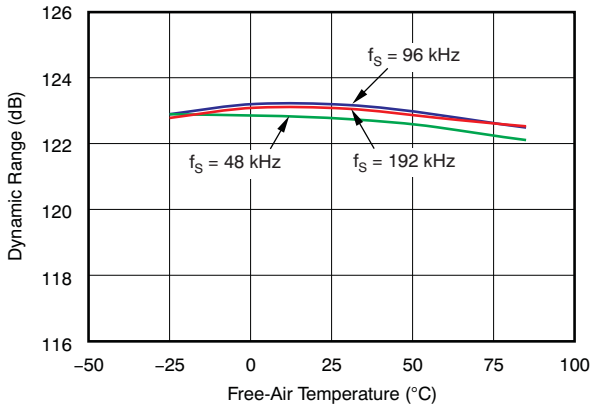


Figure 17. Dynamic Range vs Free-Air Temperature

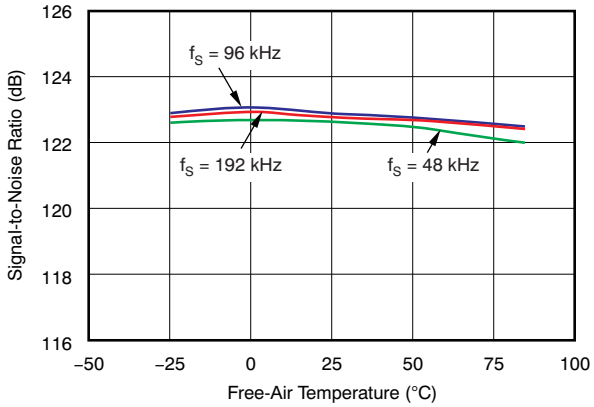


Figure 18. SNR vs Free-Air Temperature

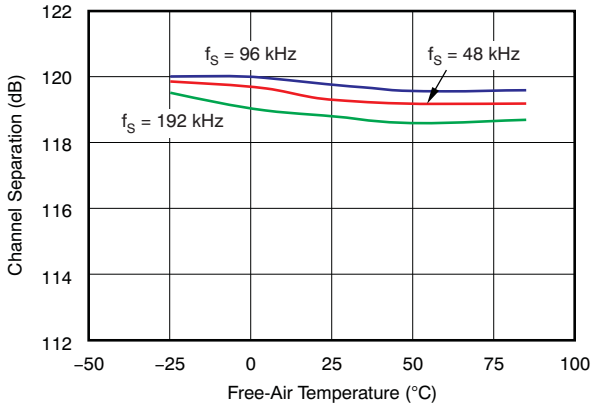


Figure 19. Channel Separation vs Free-Air Temperature

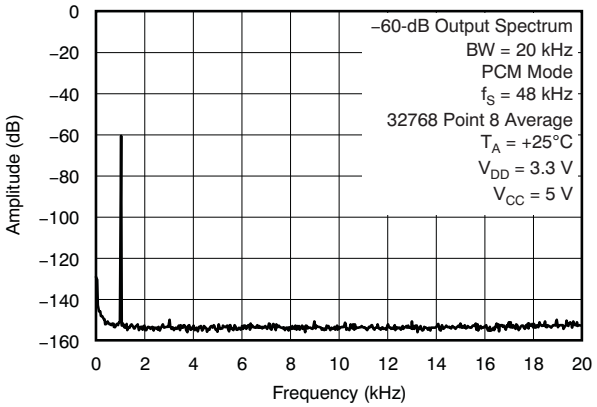


Figure 20. Amplitude vs Frequency (Measurement Circuit: Figure 53)

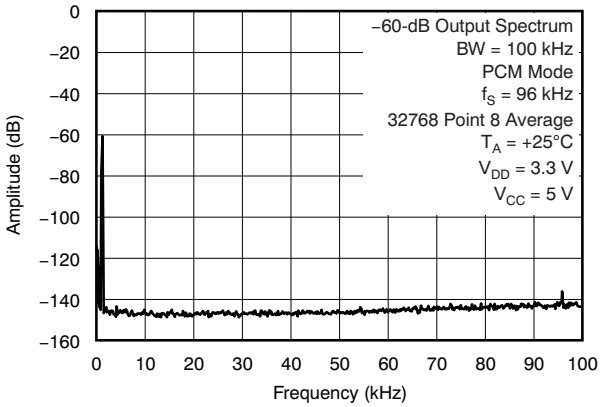


Figure 21. Amplitude vs Frequency (Measurement Circuit: Figure 53)

Analog Dynamic Performance: Temperature Characteristics (continued)

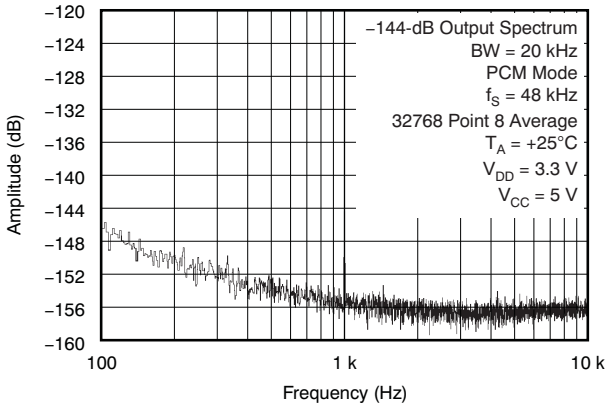


Figure 22. Amplitude vs Frequency (Measurement Circuit: Figure 53)

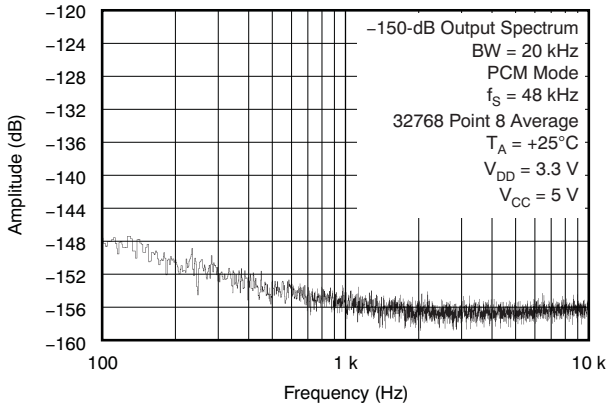


Figure 23. Amplitude vs Frequency (Measurement Circuit: Figure 53)

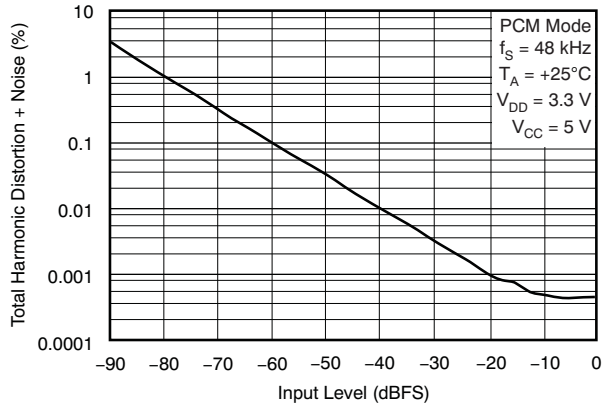


Figure 24. THD+N vs Input Level (Measurement Circuit: Figure 53)

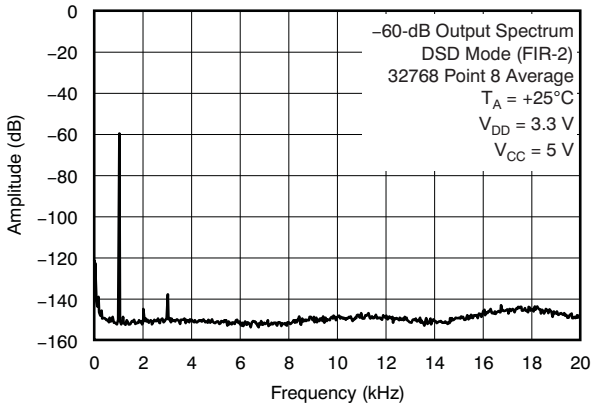


Figure 25. Amplitude vs Frequency (Measurement Circuit: Figure 54)

6.7.5 Analog FIR Filter performance in DSD Mode

All specifications at DBCK = 2.8224 MHz (44.1 kHz × 64 f_S), and 50% modulation DSD data input, unless otherwise noted.

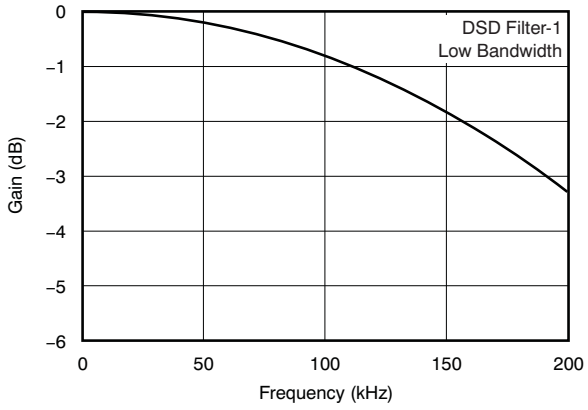


Figure 26. Gain vs Frequency

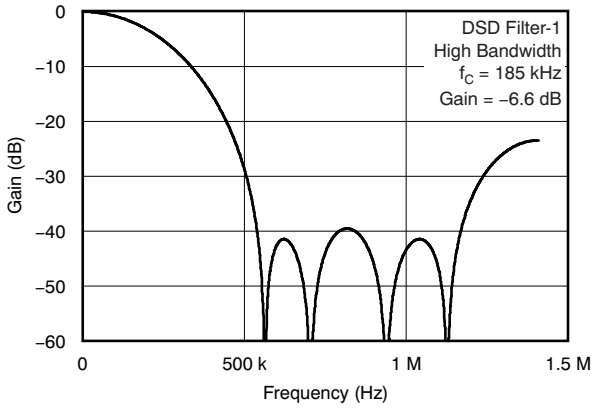


Figure 27. Gain vs Frequency (1)

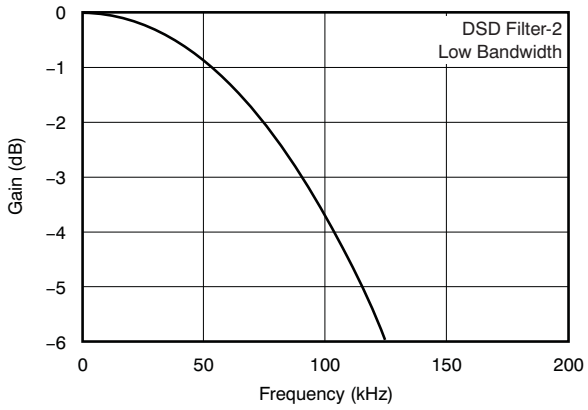


Figure 28. Gain vs Frequency

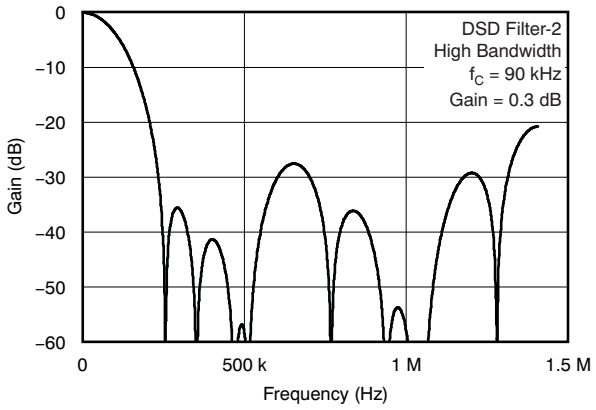


Figure 29. Gain vs Frequency

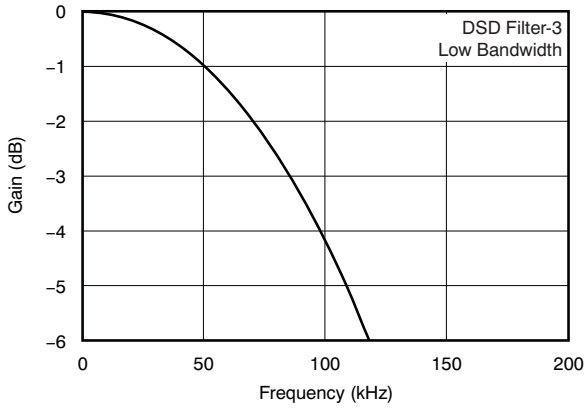


Figure 30. Gain vs Frequency

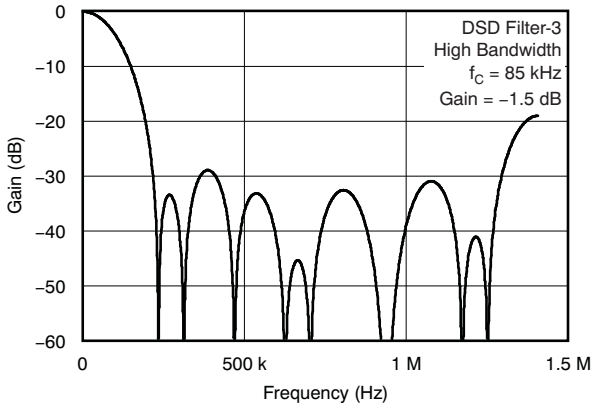


Figure 31. Gain vs Frequency

(1) This gain is in comparison to PCM 0 dB, when the DSD input signal efficiency is 50%.

Analog FIR Filter performance in DSD Mode (continued)

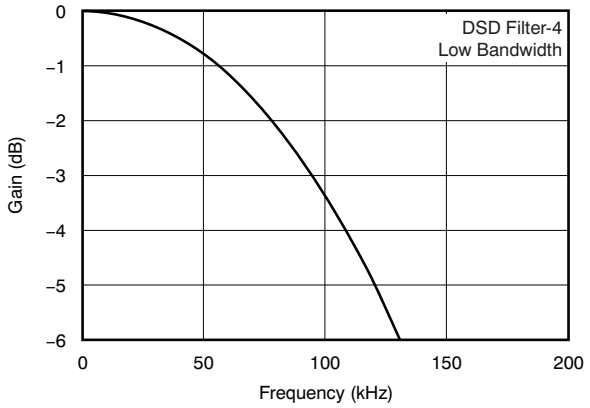


Figure 32. Gain vs Frequency

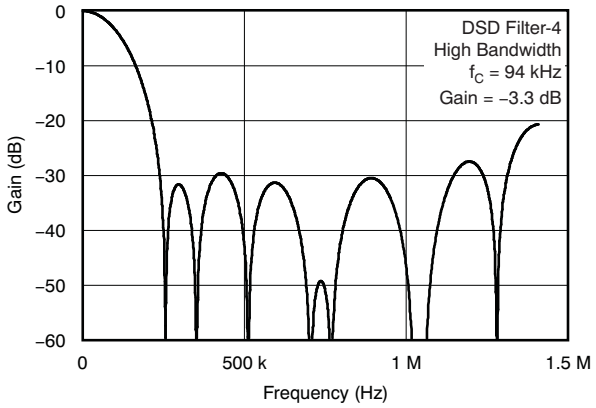


Figure 33. Gain vs Frequency

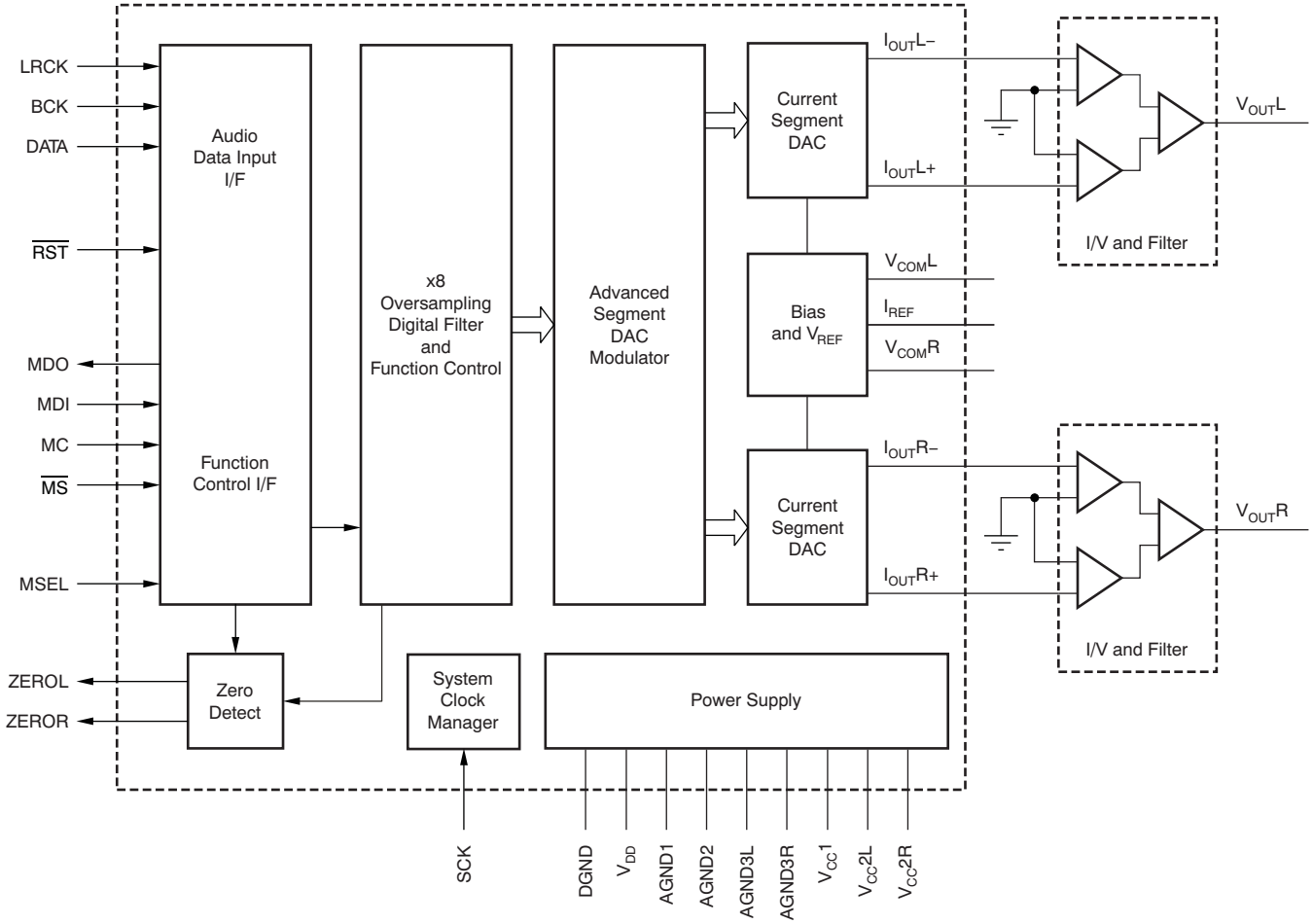
7 Detailed Description

7.1 Overview

The PCM1795 is a 32-bit, 192 kHz, differential current output stereo DAC that comes in a 28-pin SSOP package. The PCM1795 device is software controlled through I^2C or SPI, and utilizes the advanced segment DAC architecture from TI in order to perform with a Stereo Dynamic Range of 123 dB (126 dB Mono) and SNR of 123 dB (126 dB Mono) with a THD of 0.0005%. The balanced current outputs allow the user to customize the analog performance externally.

The PCM1795 device will use the SCK input as its system clock and automatically detect the sampling rate of the digital audio input and has a high tolerance for clock jitter. The PCM1795 device supports both PCM and DSD formats for audio input along with the TDMA or time-division-multiplexed command and audio-data format. The internal filter can be bypassed to allow for an external digital filter to be used.

7.2 Functional Block Diagram



7.3 Feature Description

7.3.1 Audio Data Interface

7.3.1.1 Audio Serial Interface

The audio interface port is a three-wire serial port. It includes LRCK (pin 4), BCK (pin 6), and DATA (pin 5). BCK is the serial audio bit clock, and it is used to clock the serial data present on DATA into the serial shift register of the audio interface. Serial data are clocked into the PCM1795 on the rising edge of BCK. LRCK is the serial audio left/right word clock.

The PCM1795 device requires the synchronization of LRCK and the system clock, but does not need a specific phase relation between LRCK and the system clock.

If the relationship between LRCK and the system clock changes more than ±6 BCK, internal operation is initialized within $1/f_S$ and analog outputs are forced to the bipolar zero level until resynchronization between LRCK and the system clock is completed.

7.3.1.2 PCM Audio Data Formats and Timing

The PCM1795 device supports industry-standard audio data formats, including standard right-justified, I^2S, and left-justified. The data formats are illustrated in Figure 35 to Figure 37. Data formats are selected using the format bits, FMT[2:0], in control register 18. The default data format is 32-bit I^2S. All formats require binary twos complement, MSB-first audio data. Figure 34 and Table 1 show a detailed timing diagram for the serial audio interface.

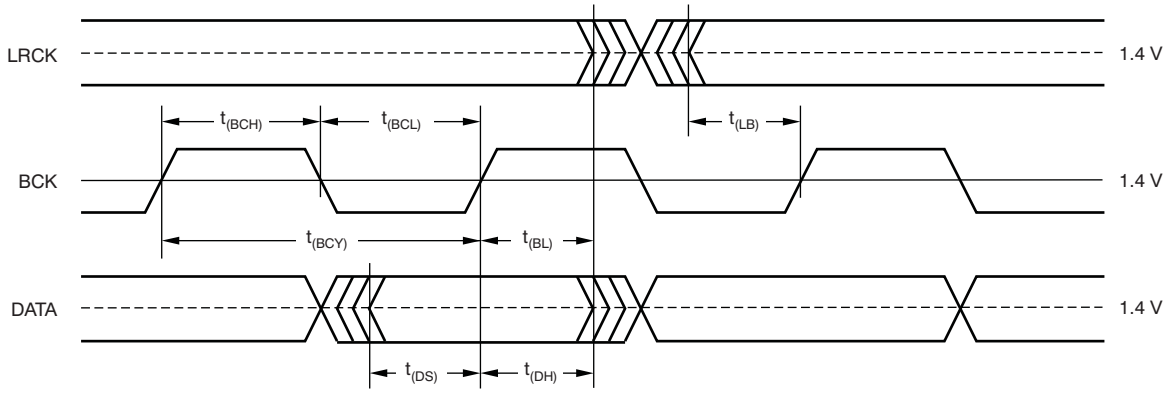


Figure 34. Audio Interface Timing

Table 1. Serial Audio Interface Timing Characteristics for Figure 34

		MIN	MAX	UNIT
$t_{(BCY)}$	BCK pulse cycle time	70		ns
$t_{(BCL)}$	BCK pulse duration, low	30		ns
$t_{(BCH)}$	BCK pulse duration, high	30		ns
$t_{(BL)}$	BCK rising edge to LRCK edge	10		ns
$t_{(LB)}$	LRCK edge to BCK rising edge	10		ns
$t_{(DS)}$	DATA setup time	10		ns
$t_{(DH)}$	DATA hold time	10		ns
	LRCK clock data	50% ± 2 bit clocks		

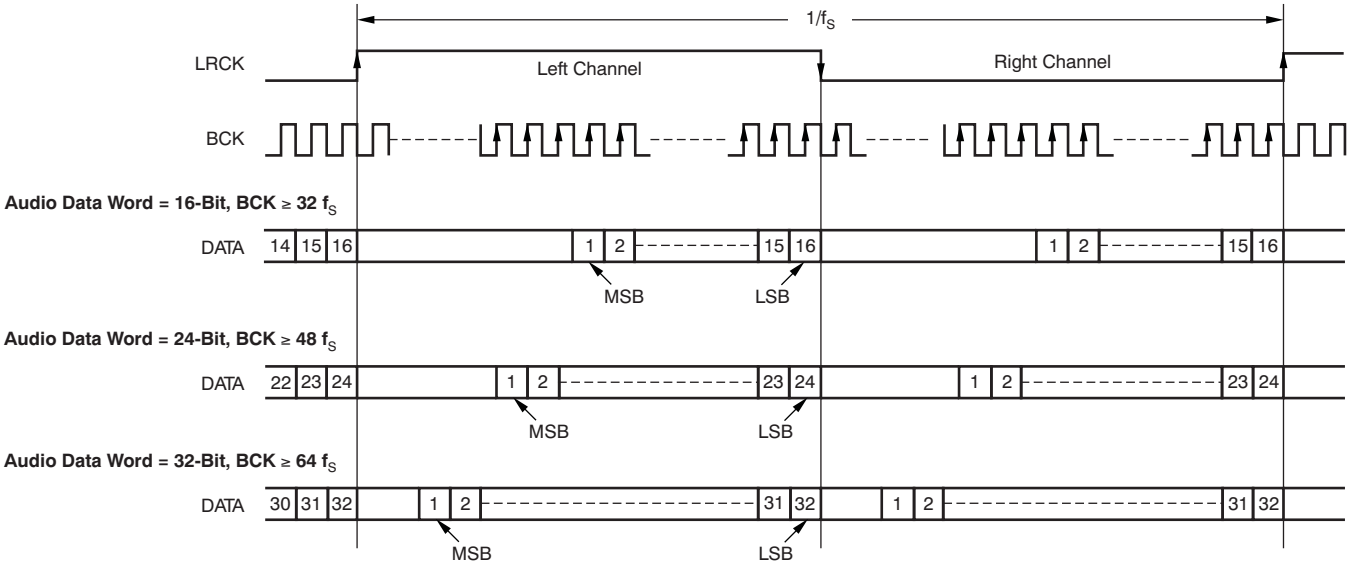


Figure 35. Audio Data Input Format: Standard Data Format (Right-Justified), Left Channel = High, Right Channel = Low

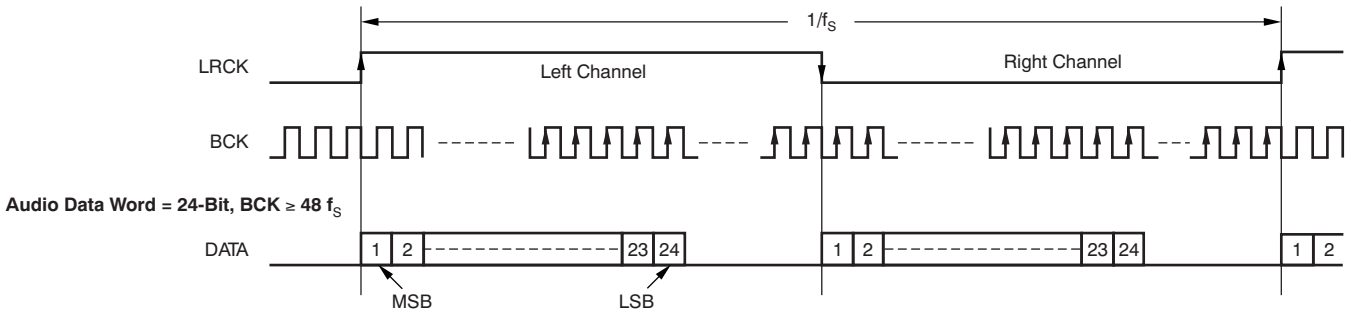


Figure 36. Audio Data Input Format: Left-Justified Data Format, Left Channel = High, Right Channel = Low

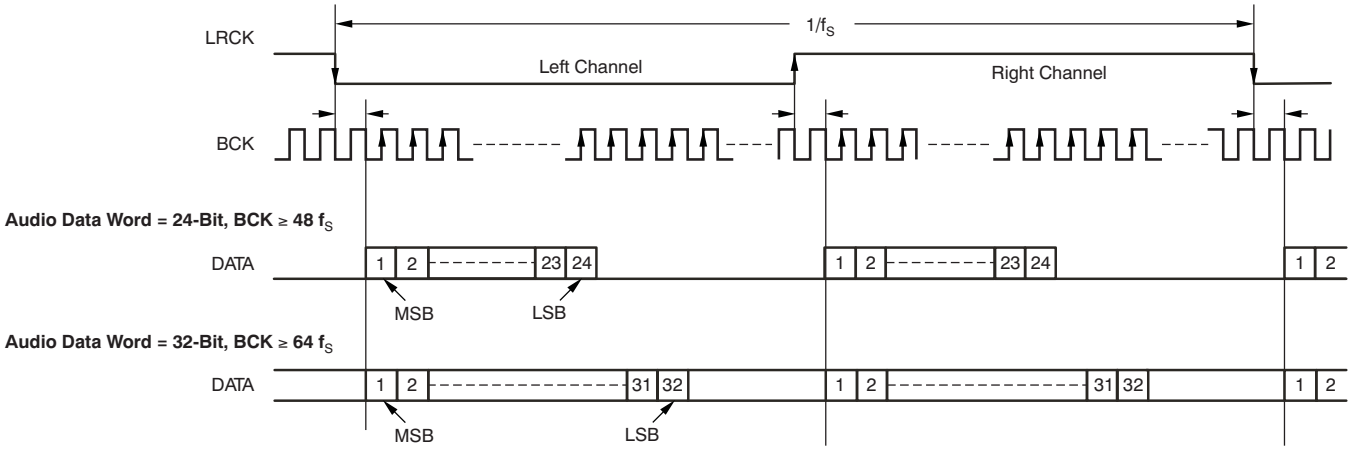


Figure 37. Audio Data Input Format: I²S Data Format, Left Channel = Low, Right Channel = High

7.3.1.3 External Digital Filter Interface and Timing

The PCM1795 device supports an external digital filter interface that consists of a three- or four-wire synchronous serial port that allows the use of an external digital filter. External filters include the Texas Instruments' DF1704 and DF1706, the Pacific Microsonics PMD200, or a programmable digital signal processor.

In the external DF mode, LRCK (pin 4), BCK (pin 6) and DATA (pin 5) are defined as: WDCK, the word clock; BCK, the bit clock; and DATA, the monaural data. The external digital filter interface is selected by using the DFTH bit of control register 20, which functions to bypass the internal digital filter of the PCM1795 device .

When the DFMS bit of control register 19 is set, the PCM1795 device can process stereo data. In this case, ZEROL (pin 1) and ZEROR (pin 2) are defined as left-channel data and right-channel data input, respectively.

Detailed information for the external digital filter interface mode is provided in *Application For External Digital Filter Interface*.

7.3.1.4 Direct Stream Digital (DSD) Format Interface and Timing

The PCM1795 device supports the DSD format interface operation, which includes out-of-band noise filtering using an internal analog FIR filter. For DSD operation, SCK (pin 7) is redefined as BCK, DATA (pin 5) as DATAL (left channel audio data), and LRCK (pin 4) as DATAR (right channel audio data). BCK (pin 6) must be forced low in the DSD mode. The DSD format interface is activated by setting the DSD bit of control register 20.

Detailed information for the DSD mode is provided in *Application For DSD Format (DSD Mode) Interface*.

7.3.1.5 TDMCA Interface

The PCM1795 device supports the time-division-multiplexed command and audio (TDMCA) data format to enable control of and communication with a number of external devices over a single serial interface.

Detailed information for the TDMCA format is provided in *TDMCA Interface Format*.

7.3.1.6 Analog Output

Table 2 and Figure 38 show the relationship between the digital input code and analog output.

Table 2. Analog Output Current and Voltage(1)

PARAMETER	800000 (–FS)	000000 (BPZ)	7FFFFF (+FS)
$I_{OUT}N$ (mA)	–1.5	–3.5	–5.5
$I_{OUT}P$ (mA)	–5.5	3.5	–1.5
$V_{OUT}N$ (V)	–1.23	–2.87	–4.51
$V_{OUT}P$ (V)	–4.51	–2.87	–1.23
V_{OUT} (V)	–2.91	0	2.91

(1) $V_{OUT}N$ is the output of U1, $V_{OUT}P$ is the output of U2, and V_{OUT} is the output of U3 in the measurement circuit of Figure 53.

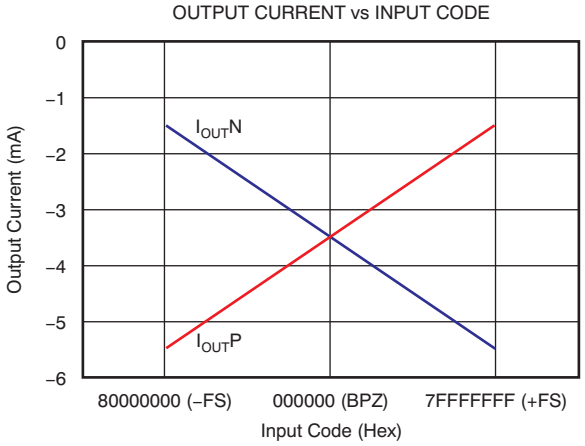


Figure 38. Relationship Between Digital Input and Analog Output

7.4 Device Functional Modes

- SPI Mode is selected by connecting MSEL to DGND. SPI mode uses four signal lines and allows higher speed full-duplex communication between the host and the PCM1795 device.
- I^2C Mode is selected by connecting MSEL to V_{DD}. I^2C uses two signal lines for half-duplex communication, and used in a variety of devices.
- I^2S input Mode is selected by default and is controlled by Register 20 bit 5.
- DSD input Mode is selected by setting Register 20 bit 5 high.
- TDMCA Mode is enabled when the PCM1795 device receives an LRCK signal with a pulse duration of two BCK clocks.

7.5 Programming

7.5.1 System Clock and Reset Functions

7.5.1.1 System Clock Input

The PCM1795 requires a system clock to operate the digital interpolation filters and advanced segment DAC modulators. The system clock is applied at the SCK input (pin 7). The PCM1795 has a system clock detection circuit that automatically senses the frequency at which the system clock is operating. Table 3 shows examples of system clock frequencies for common audio sampling rates. If the oversampling rate of the delta-sigma (ΔΣ) modulator is selected as 128 f_S, the system clock frequency is required to be greater than 256 f_S.

Figure 39 and Table 4 show the timing requirements for the system clock input. For optimal performance, it is important to use a clock source with low phase jitter and noise. The Texas Instruments PLL1700 family of multiclock generators is an excellent choice to provide the PCM1795 system clock.

Table 3. System Clock Rates for Common Audio Sampling Frequencies

SAMPLING FREQUENCY (kHz)	SYSTEM CLOCK FREQUENCY (f_{SCK}) (MHz)					
	128 f_S	192 f_S	256 f_S	384 f_S	512 f_S	768 f_S
32	4.096(1)	6.144(1)	8.192	12.288	16.384	24.576
44.1	5.6488(1)	8.4672	11.2896	16.9344	22.5792	33.8688
48	6.144(1)	9.216	12.288	18.432	24.576	36.864
96	12.288	18.432	24.576	36.864	49.152(1)	73.728(1)
192	24.576	36.864	49.152(1)	73.728(1)	X(2)	X(2)

(1) This system clock rate is not supported in I^2C fast mode.
(2) This system clock rate is not supported for the given sampling frequency.

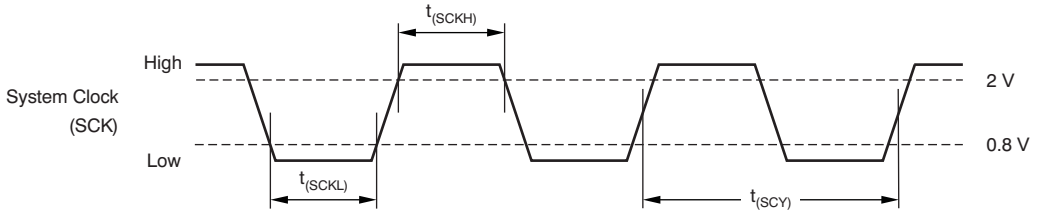


Figure 39. System Clock Input Timing

Table 4. System Clock Input Timing Characteristics for Figure 39

		MIN	MAX	UNIT
$t_{(SCY)}$	System clock pulse cycle time	13		ns
$t_{(SCKH)}$	System clock pulse duration, high	$0.4t_{(SCY)}$		ns
$t_{(SCKL)}$	System clock pulse duration, low	$0.4t_{(SCY)}$		ns

7.5.1.2 Power-On and External Reset Functions

The PCM1795 includes a power-on reset function, as shown in Figure 40. With V_{DD} > 2 V, the power-on reset function is enabled. The initialization sequence requires 1024 system clocks from the time V_{DD} > 2 V. After the initialization period, the PCM1795 is set to its default reset state, as described in *Mode Control Registers*.

The PCM1795 also includes an external reset capability using the $\overline{RST}$ input (pin 14). This feature allows an external controller or master reset circuit to force the PCM1795 to initialize to the default reset state.

Figure 41 and Table 5 show the external reset operation and timing. The $\overline{RST}$ pin is set to logic 0 for a minimum of 20 ns. The $\overline{RST}$ pin is then set to a logic 1 state, thus starting the initialization sequence that requires 1024 system clock periods. The external reset is especially useful in applications where there is a delay between the PCM1795 power-up and system clock activation.

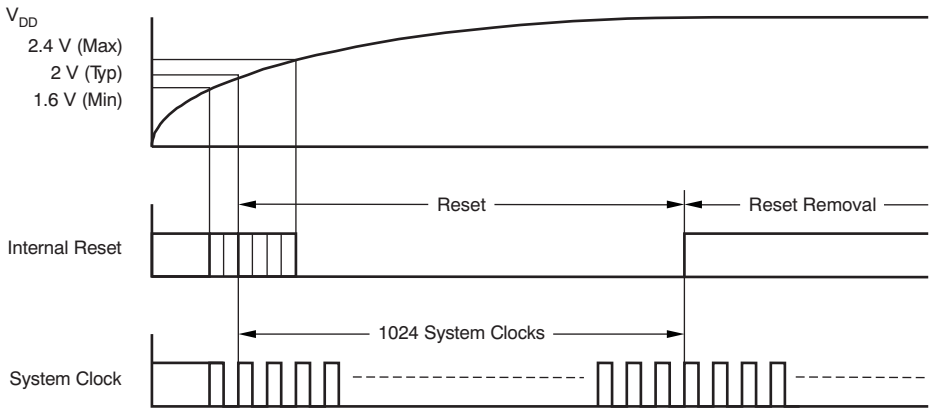


Figure 40. Power-On Reset Timing

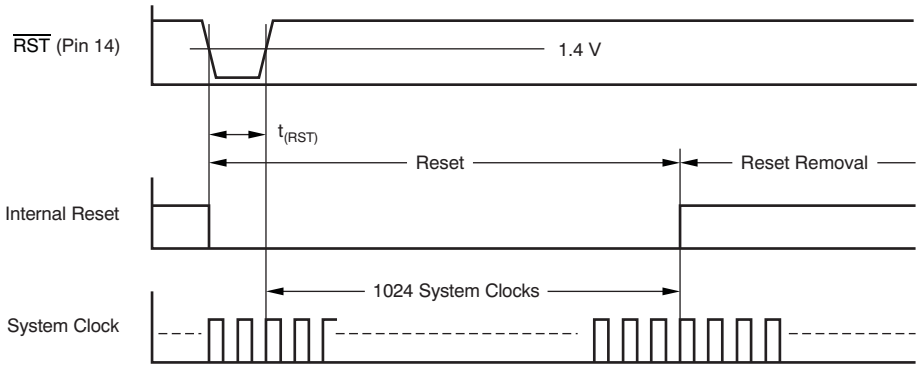


Figure 41. External Reset Timing

Table 5. External Reset Timing Characteristics for Figure 41

		MIN	MAX	UNIT
$t_{(RST)}$	Reset pulse duration, low	20		ns

7.5.2 Function Descriptions

7.5.2.1 Zero Detect

The PCM1795 has a zero-detect function. When the PCM1795 detects the zero conditions as shown in Table 6, the PCM1795 sets ZEROL (pin 1) and ZEROR (pin 2) high.

Table 6. Zero Conditions

MODE		DETECTING CONDITION AND TIME
PCM		DATA is continuously low for 1024 LRCKs.
External DF mode		DATA is continuously low for 1024 WDCKs.
DSD	DZ0	There are an equal number of 1s and 0s in every 8 bits of DSD input data for 23 ms.
	DZ1	The input data are continuously 1001 0110 for 23 ms.

7.5.3 Serial Control Interface

The PCM1795 supports both SPI and I^2C interfaces that set the mode control registers; see Table 10. The serial control interface is selected by MSEL (pin 3); SPI is activated when MSEL is set low, and I^2C is activated when MSEL is set high.

7.5.3.1 SPI Interface

The SPI interface is a four-wire synchronous serial port that operates asynchronously to the serial audio interface and the system clock (SCK). The serial control interface is used to program and read the on-chip mode registers. The control interface includes MDO (pin 13), MDI (pin 11), MC (pin 12), and $\overline{MS}$ (pin 10). MDO is the serial data output, used to read back the values of the mode registers; MDI is the serial data input, used to program the mode registers; MC is the serial bit clock, used to shift data in and out of the control port; and $\overline{MS}$ is the mode control enable, used to enable the internal mode register access.

7.5.3.2 Register Read/Write Operation

All read/write operations for the serial control port use 16-bit data words. Figure 42 shows the control data word format. The most significant bit (MSB) is the read/write (R/$\overline{W}$) bit. For write operations, the R/$\overline{W}$ bit must be set to '0'. For read operations, the R/$\overline{W}$ bit must be set to '1'. There are 7 bits, labeled IDX[6:0], that hold the register index (or address) for the read and write operations. The least significant 8 bits, D[7:0], contain the data to be written to, or the data that was read from, and the register specified by IDX[6:0].

Figure 43 shows the functional timing diagram for writing or reading the serial control port. $\overline{MS}$ is held at a logic 1 state until a register must be written to or read from. To start the register write or read cycle, $\overline{MS}$ is set to logic 0. Sixteen clocks are then provided on MC, corresponding to the 16 bits of the control data word on MDI and readback data on MDO. After the eighth clock cycle has completed, the data from the indexed-mode control register appears on MDO during the read operation. After the 16th clock cycle has completed, the data are latched into the indexed-mode control register during the write operation. To write or read subsequent data, $\overline{MS}$ must be set to '1' once.

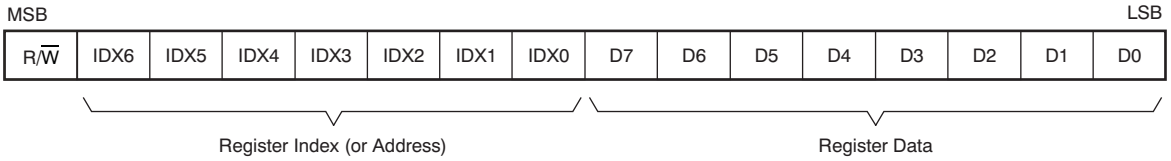
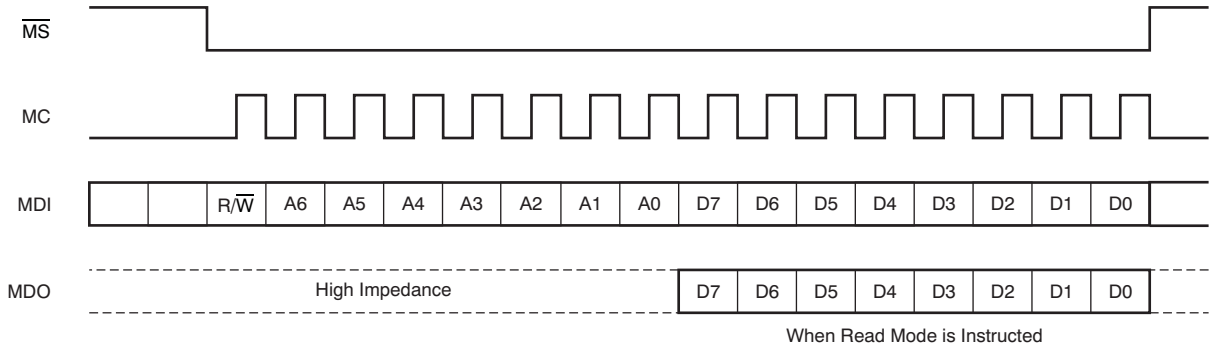


Figure 42. Control Data Word Format for MDI



NOTE: Bit 15 is used for selection of write or read. Setting R/$\overline{W}$ = 0 indicates a write, while R/$\overline{W}$ = 1 indicates a read. Bits 14–8 are used for the register address. Bits 7–0 are used for register data.

Figure 43. Serial Control Format

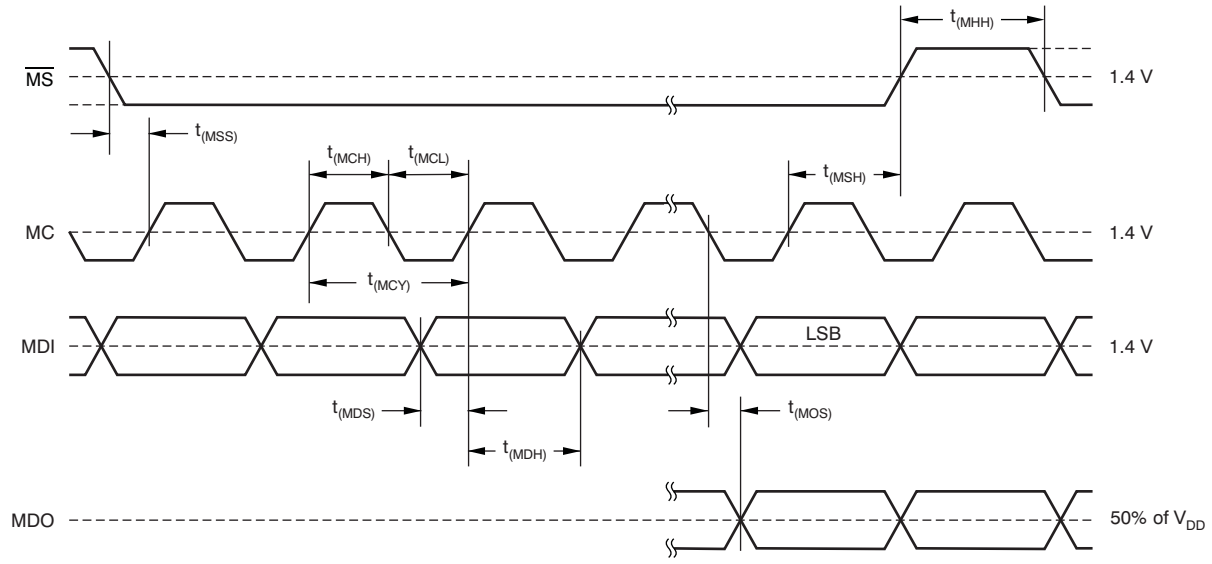


Figure 44. Control Interface Timing

Table 7. Control Interface Timing Characteristics for Figure 44

		MIN	MAX	UNIT
$t_{(MCY)}$	MC pulse cycle time	100		ns
$t_{(MCL)}$	MC low-level time	40		ns
$t_{(MCH)}$	MC high-level time	40		ns
$t_{(MHH)}$	$\overline{MS}$ high-level time	80		ns
$t_{(MSS)}$	$\overline{MS}$ falling edge to MC rising edge	15		ns
$t_{(MSH)}$	$\overline{MS}$ hold time(1)	15		ns
$t_{(MDH)}$	MDI hold time	15		ns
$t_{(MDS)}$	MDI setup time	15		ns
$t_{(MOS)}$	MC falling edge to MDO stable		30	ns

(1) MC rising edge for LSB to $\overline{MS}$ rising edge.

7.5.4 I²C Interface

The PCM1795 supports the I²C serial bus and the data transmission protocol for standard and fast mode as a slave device. This protocol is explained in the I²C specification 2.0.

In I²C mode, the control terminals are changed as described in Table 8.

Table 8. Control Terminals

TERMINAL NAME	TDMCA NAME	PROPERTY	DESCRIPTION
$\overline{MS}$	ADR0	Input	I²C address 0
MDI	ADR1	Input	I²C address 1
MC	SCL	Input	I²C clock
MDO	SDA	Input/output	I²C data

7.5.4.1 Slave Address

The PCM1795 has 7 bits for its own slave address, as shown in Figure 45. The first 5 bits (MSBs) of the slave address are factory preset to *10011*. The next 2 bits of the address byte are the device select bits that can be user-defined by the ADR1 and ADR0 terminals. A maximum of four PCM1795 devicess can be connected on the same bus at one time. Each PCM1795 responds when it receives its own slave address.

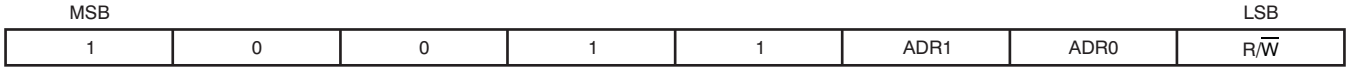


Figure 45. Slave Address

7.5.4.2 Packet Protocol

A master device must control packet protocol that consists of a start condition, slave address, read/write bit, data if write or acknowledge if read, and stop condition. The PCM1795 supports only slave receivers and slave transmitters.

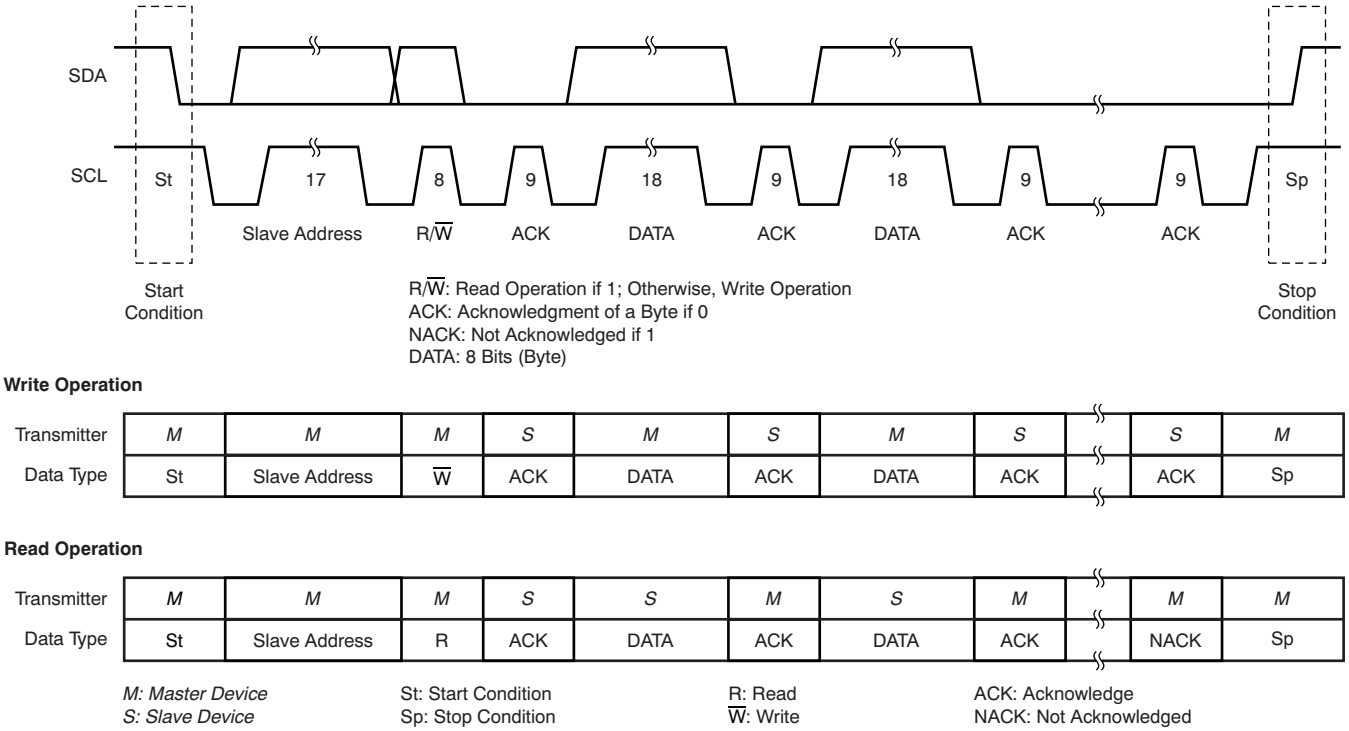


Figure 46. Basic I²C Framework

7.5.4.3 Write Register

A master can write to any PCM1795 registers using single or multiple accesses. The master sends a PCM1795 slave address with a write bit, a register address, and the data. If multiple access is required, the address is that of the starting register, followed by the data to be transferred. When the data are received properly, the index register is incremented by '1' automatically. When the index register reaches 0x7F, the next value is 0x00. When undefined registers are accessed, the PCM1795 does not send an acknowledgment. Figure 47 shows a diagram of the write operation.

Transmitter	M	M	M	S	M	S	M	S	M	S		S	M
Data Type	St	Slave Address	$\overline{W}$	ACK	Register Address	ACK	Write Data 1	ACK	Write Data 2	ACK		NACK	Sp

M: Master Device
S: Slave Device
St: Start Condition
Sp: Stop Condition
ACK: Acknowledge
NACK: Not Acknowledged
$\overline{W}$: Write

Figure 47. Write Operation

7.5.4.4 Read Register

A master can read the PCM1795 register. The value of the register address is stored in an indirect index register in advance. The master sends a PCM1795 slave address with a read bit after storing the register address. Then the PCM1795 transfers the data that the index register points to. When the data are transferred during a multiple access, the index register is incremented by '1' automatically. (When first going into read mode immediately following a write, the index register is not incremented. The master can read the register that was previously written.) When the index register reaches 0x7F, the next value is 0x00. The PCM1795 outputs some data when the index register is 0x10 to 0x1F, even if it is not defined in Table 10. Figure 48 shows a diagram of the read operation.

Transmitter	M	M	M	S	M	S	M	M	M	S	S	M		M	M
Data Type	St	Slave Address	$\overline{W}$	ACK	Register Address	ACK	Sr	Slave Address	R	ACK	Data	ACK		NACK	Sp

M: Master Device
S: Slave Device
St: Start Condition
Sr: Repeated Start Condition
Sp: Stop Condition
R: Read
$\overline{W}$: Write
ACK: Acknowledge
NACK: Not Acknowledged

Figure 48. Read Operation

7.5.4.5 Noise Suppression

The PCM1795 incorporates noise suppression using the system clock (SCK). However, there must be no more than two noise spikes in 600 ns. The noise suppression works for SCK frequencies between 8 MHz and 40 MHz in fast mode. However, it works incorrectly under the following conditions:

Case 1:

1. $t_{(SCK)} > 120$ ns ($t_{(SCK)}$: period of SCK)
2. $t_{(HI)} + t_{(D–HD)} < t_{(SCK)} \times 5$
3. Spike noise exists on the first half of the SCL high pulse.
4. Spike noise exists on the SDA high pulse just before SDA goes low.

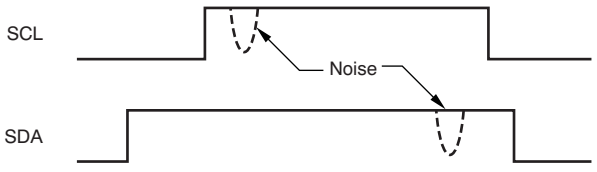


Figure 49. Case 1

When these conditions occur at the same time, the data are recognized as low.

Case 2:

1. $t_{(SCK)}$ > 120 ns
2. $t_{(S–HD)}$ or $t_{(RS–HD)}$ < $t_{(SCK)}$ × 5
3. Spike noise exists on both SCL and SDA during the hold time.

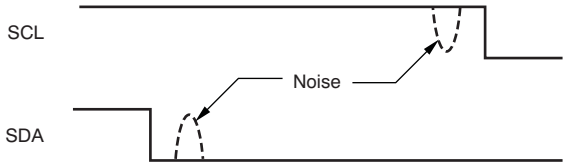


Figure 50. Case 2

When these conditions occur at the same time, the PCM1795 fails to detect a start condition.

Case 3:

1. $t_{(SCK)}$ < 50 ns
2. $t_{(SP)}$ > $t_{(SCK)}$
3. Spike noise exists on SCL just after SCL goes low.
4. Spike noise exists on SDA just before SCL goes low.

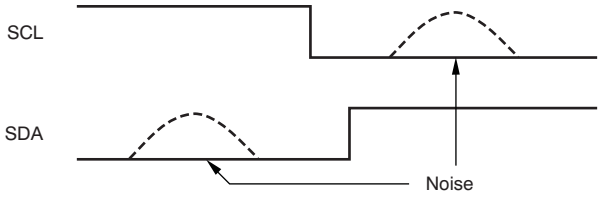


Figure 51. Case 3

When these conditions occur at the same time, the PCM1795 erroneously detects a start or stop condition.

7.6 Register Maps

7.6.1 Mode Control Registers

7.6.1.1 User-Programmable Mode Controls

The PCM1795 device includes a number of user-programmable functions that are accessed via mode control registers. The registers are programmed using the serial control interface, as previously discussed in *SPI Interface* and *I²C Interface*. Table 9 lists the available mode-control functions, along with the default reset conditions and associated register index.

Table 9. User-Programmable Function Controls

FUNCTION	DEFAULT	REGISTER	BIT	PCM	DSD	DF BYPASS
Digital attenuation control 0 dB to –120 dB and mute, 0.5-dB step	0 dB	Register 16 Register 17	ATL[7:0] (for left channel) ATR[7:0] (for right channel)	Yes	No	No
Attenuation load control Disabled, enabled	Attenuation disabled	Register 18	ATLD	Yes	No	No
Input audio data format selection 16-, 20-, 32-bit standard (right-justified) format 24-bit MSB-first left-justified format 16-/32-bit I²S format	24-bit I²S format	Register 18	FMT[2:0]	Yes	No	Yes

Register Maps (continued)

Table 9. User-Programmable Function Controls (continued)

FUNCTION	DEFAULT	REGISTER	BIT	PCM	DSD	DF BYPASS
Sampling rate selection for de-emphasis Disabled, 44.1 kHz, 48 kHz, 32 kHz	De-emphasis disabled	Register 18	DMF[1:0]	Yes	Yes(1)	No
De-emphasis control Disabled, enabled	De-emphasis disabled	Register 18	DME	Yes	No	No
Soft mute control Soft mute disabled, enabled	Mute disabled	Register 18	MUTE	Yes	No	No
Output phase reversal Normal, reverse	Normal	Register 19	REV	Yes	Yes	Yes
Attenuation speed selection $\times 1 f_S$, $\times (1/2) f_S$, $\times (1/4) f_S$, $\times (1/8) f_S$	$\times 1 f_S$	Register 19	ATS[1:0]	Yes	No	No
DAC operation control Enabled, disabled	DAC operation enabled	Register 19	OPE	Yes	Yes	Yes
Stereo DF bypass mode select Monaural, stereo	Monaural	Register 19	DFMS	Yes	No	Yes
Digital filter roll-off selection Sharp roll-off, slow roll-off	Sharp roll-off	Register 19	FLT	Yes	No	No
Infinite zero mute control Disabled, enabled	Disabled	Register 19	INZD	Yes	No	Yes
System reset control Reset operation, normal operation	Normal operation	Register 20	SRST	Yes	Yes	Yes
DSD interface mode control DSD enabled, disabled	Disabled	Register 20	DSD	Yes	Yes	No
Digital-filter bypass control DF enabled, DF bypass	DF enabled	Register 20	DFTH	Yes	No	Yes
Monaural mode selection Stereo, monaural	Stereo	Register 20	MONO	Yes	Yes	Yes
Channel selection for monaural mode data Left channel, Right channel	Left channel	Register 20	CHSL	Yes	Yes	Yes
ΔΣ oversampling rate selection $\times 64 f_S$, $\times 128 f_S$, $\times 32 f_S$	$\times 64 f_S$	Register 20	OS[1:0]	Yes	Yes(2)	Yes
PCM zero output enable	Enabled	Register 21	PCMZ	Yes	No	Yes
DSD zero output enable	Disabled	Register 21	DZ[1:0]	Yes	Yes	No
FUNCTION AVAILABLE ONLY FOR READ						
Zero detection flag Not zero, zero detected	Not zero = 0 Zero detected = 1	Register 22	ZFGL (for left channel) ZFGR (for right channel)	Yes	Yes	Yes
Device ID (at TDMCA)	—	Register 23	ID[4:0]	Yes	No	No

(1) When in DSD mode, DMF[1:0] is defined as DSD filter (analog FIR) performance selection.
(2) When in DSD mode, OS[1:0] is defined as DSD filter (analog FIR) operating rate selection.

7.6.1.2 Register Map

The mode control register map is shown in Table 10. Registers 16 to 21 include an R/$\overline{W}$ bit that determines whether a register read (R/$\overline{W}$ = 1) or write (R/$\overline{W}$ = 0) operation is performed. Registers 22 and 23 are read-only.

Table 10. Mode Control Register Map

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	R/$\overline{W}$	0	0	1	0	0	0	0	ATL7	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 17	R/$\overline{W}$	0	0	1	0	0	0	1	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0
Register 18	R/$\overline{W}$	0	0	1	0	0	1	0	ATLD	FMT2	FMT1	FMT0	DMF1	DMF0	DME	MUTE
Register 19	R/$\overline{W}$	0	0	1	0	0	1	1	REV	ATS1	ATS0	OPE	RSV	DFMS	FLT	INZD

Table 10. Mode Control Register Map (continued)

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 20	R/$\overline{W}$	0	0	1	0	1	0	0	RSV	SRST	DSD	DFTH	MONO	CHSL	OS1	OS0
Register 21	R/$\overline{W}$	0	0	1	0	1	0	1	RSV	RSV	RSV	RSV	RSV	DZ1	DZ0	PCMZ
Register 22	R	0	0	1	0	1	1	0	RSV	RSV	RSV	RSV	RSV	RSV	ZFGR	ZFGL
Register 23	R	0	0	1	0	1	1	1	RSV	RSV	RSV	ID4	ID3	ID2	ID1	ID0

7.6.1.3 Register Definitions

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	R/$\overline{W}$	0	0	1	0	0	0	0	ATL7	ATL6	ATL5	ATL4	ATL3	ATL2	ATL1	ATL0
Register 17	R/$\overline{W}$	0	0	1	0	0	0	1	ATR7	ATR6	ATR5	ATR4	ATR3	ATR2	ATR1	ATR0

7.6.1.3.1 R/$\overline{W}$: Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

7.6.1.3.2 ATx[7:0]: Digital Attenuation Level Setting

These bits are available for read and write.

Default value: 1111 1111b

Each DAC output has a digital attenuator associated with it. The attenuator can be set from 0 dB to –120 dB, in 0.5-dB steps. Alternatively, the attenuator can be set to infinite attenuation (or mute). The attenuation data for each channel can be set individually. However, the data load control (the ATLD bit of control register 18) is common to both attenuators. ATLD must be set to '1' in order to change an attenuator setting. The attenuation level can be set using Equation 1.

Attenuation level (dB) = 0.5 dB × (ATx[7:0]$_{DEC}$ – 255)

where

ATx[7:0]$_{DEC}$ = 0 through 255 (1)

For ATx[7:0]$_{DEC}$ = 0 through 14, the attenuator is set to infinite attenuation. Table 11 lists the attenuation levels for various settings.

Table 11. Attenuation Levels

ATx[7:0]	DECIMAL VALUE	ATTENUATION LEVEL SETTING
1111 1111b	255	0 dB, no attenuation (default)
1111 1110b	254	–0.5 dB
1111 1101b	253	–1.0 dB
—	—	—
0001 0000b	16	–119.5 dB
0000 1111b	15	–120.0 dB
0000 1110b	14	Mute
—	—	—
0000 0000b	0	Mute

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 18	R/$\overline{W}$	0	0	1	0	0	1	0	ATLD	FMT2	FMT1	FMT0	DMF1	DMF0	DME	MUTE

7.6.1.3.3 R/$\overline{W}$: Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

7.6.1.3.4 ATLD: Attenuation Load Control

This bit is available for read and write.

Default value: 0

Table 12. ATLD

ATLD	ATTENUATION CONTROL SETTING
ATLD = 0	Attenuation control disabled (default)
ATLD = 1	Attenuation control enabled

The ATLD bit is used to enable loading of the attenuation data contained in registers 16 and 17. When ATLD = 0, the attenuation settings remain at the previously programmed levels, ignoring new data loaded from registers 16 and 17. When ATLD = 1, attenuation data written to registers 16 and 17 is loaded normally.

7.6.1.3.5 FMT[2:0]: Audio Interface Data Format

These bits are available for read and write.

Default value: 101

Table 13. FMT[2:0]

FMT[2:0]	AUDIO DATA FORMAT SELECTION
000	16-bit standard format, right-justified data, BCK ≥ x32 f_S
001	32-bit standard format, right-justified data, BCK ≥ x64 f_S
010	24-bit standard format, right-justified data, BCK ≥ x48 f_S
011	24-bit MSB-first, left-justified format data, BCK ≥ x48 f_S
100	32-bit I^2S format data, BCK ≥ x64 f_S
101	24-bit I^2S format data (default), BCK ≥ x48 f_S
110	Reserved
111	Reserved

The FMT[2:0] bits are used to select the data format for the serial audio interface.

For the external digital filter interface mode (DFTH mode), this register is operated as shown in *Application for External Digital Filter Interface*.

7.6.1.3.6 DMF[1:0]: Sampling Frequency Selection for the De-Emphasis Function

These bits are available for read and write.

Default value: 00

Table 14. DMF[1:0]

DMF[1:0]	DE-EMPHASIS SAMPLING FREQUENCY SELECTION
00	Disabled (default)
01	48 kHz
10	44.1 kHz
11	32 kHz

The DMF[1:0] bits are used to select the sampling frequency used by the digital de-emphasis function when it is enabled by setting the DME bit. The de-emphasis curves are shown in *Typical Characteristics*.

For the DSD mode, analog FIR filter performance can be selected using this register. A register map and filter response plots are shown in *Application For DSD Format (DSD Mode) Interface*.

7.6.1.3.7 DME: Digital De-Emphasis Control

This bit is available for read and write.

Default value: 0

Table 15. DME

DME	DE-EMPHASIS SETTING
DME = 0	De-emphasis disabled (default)
DME = 1	De-emphasis enabled

The DME bit is used to enable or disable the de-emphasis function for both channels.

7.6.1.3.8 MUTE: Soft Mute Control

This bit is available for read and write.

Default value: 0

Table 16. MUTE

MUTE	SOFT MUTE SETTING
MUTE = 0	Soft mute disabled (default)
MUTE = 1	Soft mute enabled

The MUTE bit is used to enable or disable the soft mute function for both channels.

Soft mute is operated as a 256-step attenuator. The speed for each step to –∞ dB (mute) is determined by the attenuation rate selected in the ATS register.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 19	R/$\overline{W}$	0	0	1	0	0	1	1	REV	ATS1	ATS0	OPE	RSV	DMFS	FLT	INZD

7.6.1.3.9 R/$\overline{W}$: Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

7.6.1.3.10 REV: Output Phase Reversal

This bit is available for read and write.

Default value: 0

Table 17. REV

REV	OUTPUT SETTING
REV = 0	Normal output (default)
REV = 1	Inverted output

The REV bit is used to invert the output phase for both channels.

7.6.1.3.11 ATS[1:0]: Attenuation Rate Select

These bits are available for read and write.

Default value: 00

Table 18. ATS[1:0]

ATS[1:0]	ATTENUATION RATE SELECTION
00	Every LRCK (default)
01	LRCK/2
10	LRCK/4
11	LRCK/8

The ATS[1:0] bits are used to select the rate at which the attenuator is decremented/incremented during level transitions.

7.6.1.3.12 OPE: DAC Operation Control

This bit is available for read and write.

Default value: 0

Table 19. OPE

OPE	DAC OPERATION CONTROL
OPE = 0	DAC operation enabled (default)
OPE = 1	DAC operation disabled

The OPE bit is used to enable or disable the analog output for both channels. Disabling the analog outputs forces them to the bipolar zero level (BPZ) even if audio data are present on the input.

7.6.1.3.13 DFMS: Stereo DF Bypass Mode Select

This bit is available for read and write.

Default value: 0

Table 20. DFMS

DFMS	MODE SELECTION
DFMS = 0	Monaural (default)
DFMS = 1	Stereo input enabled

The DFMS bit is used to enable stereo operation in DF bypass mode. In the DF bypass mode, when DFMS is set to '0', the pin for the input data are DATA (pin 5) only; therefore, the PCM1795 operates as a monaural DAC. When DFMS is set to '1', the PCM1795 can operate as a stereo DAC with inputs of the left channel and right channel data on ZEROL (pin 1) and ZEROR (pin 2), respectively.

7.6.1.3.14 FLT: Digital Filter Roll-Off Control

This bit is available for read and write.

Default value: 0

Table 21. FLT

FLT	ROLL-OFF CONTROL
FLT = 0	Sharp roll-off (default)
FLT = 1	Slow roll-off

The FLT bit is used to select the digital filter roll-off characteristic. The filter responses for these selections are shown in *Typical Characteristics*.

7.6.1.3.15 INZD: Infinite Zero Detect Mute Control

This bit is available for read and write.

Default value: 0

Table 22. INZD

INZD	INFINITE ZERO DETECT MUTE SETTING
INZD = 0	Infinite zero detect mute disabled (default)
INZD = 1	Infinite zero detect mute enabled

The INZD bit is used to enable or disable the zero detect mute function. Setting INZD to '1' forces muted analog outputs to hold a bipolar zero level when the PCM1795 detects a zero condition in both channels. The infinite zero detect mute function is not available in the DSD mode.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 20	R/$\overline{W}$	0	0	1	0	1	0	0	RSV	SRST	DSD	DFTH	MONO	CHSL	OS1	OS0

7.6.1.3.16 R/$\overline{W}$: Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

7.6.1.3.17 SRST: System Reset Control

This bit is available for write only.

Default value: 0

Table 23. SRST

SRST	SYSTEM RESET CONTROL
SRST = 0	Normal operation (default)
SRST = 1	System reset operation (generate one reset pulse)

The SRST bit is used to reset the PCM1795 to the initial system condition.

7.6.1.3.18 DSD: DSD Interface Mode Control

This bit is available for read and write.

Default value: 0

Table 24. DSD

DSD	DSD INTERFACE MODE CONTROL
DSD = 0	DSD interface mode disabled (default)
DSD = 1	DSD interface mode enabled

The DSD bit is used to enable or disable the DSD interface mode.

7.6.1.3.19 DFTH: Digital Filter Bypass (or Through Mode) Control

This bit is available for read and write.

Default value: 0

Table 25. DFTH

DFTH	DIGITAL FILTER CONTROL
DFTH = 0	Digital filter enabled (default)
DFTH = 1	Digital filter bypassed for external digital filter

The DFTH bit is used to enable or disable the external digital filter interface mode.

7.6.1.3.20 MONO: Monaural Mode Selection

This bit is available for read and write.

Default value: 0

Table 26. MONO

MONO	MODE SELECTION
MONO = 0	Stereo mode (default)
MONO = 1	Monaural mode

The MONO function is used to change operation mode from the normal stereo mode to the monaural mode. When the monaural mode is selected, both DACs operate in a balanced mode for one channel of audio input data. Channel selection is available for left-channel or right-channel data, determined by the *CHSL bit*.

7.6.1.3.21 CHSL: Channel Selection for Monaural Mode

This bit is available for read and write.

Default value: 0

Table 27. CHSL

CHSL	CHANNEL SELECTION
CHSL = 0	Left channel selected (default)
CHSL = 1	Right channel selected

This bit is available when MONO = 1.

The CHSL bit selects left-channel or right-channel data to be used in monaural mode.

7.6.1.3.22 OS[1:0]: ΔΣ Oversampling Rate Selection

These bits are available for read and write.

Default value: 00

Table 28. OS[1:0]

OS[1:0]	OPERATING SPEED SELECTION
00	64 times f_S (default)
01	32 times f_S
10	128 times f_S
11	Reserved

The OS bits are used to change the oversampling rate of ΔΣ modulation. Use of this function enables the designer to stabilize the conditions at the post low-pass filter for different sampling rates. As an application example, programming to set 128 times in 44.1-kHz operation, 64 times in 96-kHz operation, or 32 times in 192-kHz operation allows the use of only a single type (cut-off frequency) of post low-pass filter. The 128-f_S oversampling rate is not available at sampling rates above 100 kHz. If the 128-f_S oversampling rate is selected, a system clock of more than 256 f_S is required.

In DSD mode, these bits are used to select the speed of the bit clock for DSD data coming into the analog FIR filter.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 21	R/$\overline{W}$	0	0	1	0	1	0	1	RSV	RSV	RSV	RSV	RSV	DZ1	DZ0	PCMZ

7.6.1.3.23 R/$\overline{W}$: Read/Write Mode Select

When R/$\overline{W}$ = 0, a write operation is performed.

When R/$\overline{W}$ = 1, a read operation is performed.

Default value: 0

7.6.1.3.24 DZ[1:0]: DSD Zero Output Enable

These bits are available for read and write.

Default value: 00

Table 29. DZ[1:0]

DZ[1:0]	ZERO OUTPUT ENABLE
00	Disabled (default)
01	Even pattern detect 1 × 96h pattern detect

The DZ bits are used to enable or disable the output zero flags and to select the zero pattern in DSD mode.

7.6.1.3.25 PCMZ: PCM Zero Output Enable

These bits are available for read and write.

Default value: 1

Table 30. PCMZ

PCMZ	PCM ZERO OUTPUT SETTING
PCMZ = 0	PCM zero output disabled
PCMZ = 1	PCM zero output enabled (default)

The PCMZ bit is used to enable or disable the output zero flags in PCM mode and the external DF mode.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 22	R	0	0	1	0	1	1	0	RSV	RSV	RSV	RSV	RSV	RSV	ZFGR	ZFGL

7.6.1.3.26 R: Read Mode Select

Value is always '1', specifying the readback mode.

7.6.1.3.27 ZFGx: Zero-Detection Flag

Where *x* = L or R, corresponding to the DAC output channel. These bits are available only for readback.

Default value: 00

Table 31. ZFGx

ZFGx	ZERO DETECTION
ZFGx = 0	Not zero
ZFGx = 1	Zero detected

These bits show zero conditions. The status is the same as that of the zero flags at ZEROL (pin 1) and ZEROR (pin 2). See *Zero Detect*.

	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 23	R	0	0	1	0	1	1	1	RSV	RSV	RSV	ID4	ID3	ID2	ID1	ID0

7.6.1.3.28 Read Mode Select

Value is always '1', specifying the readback mode.

7.6.1.3.29 ID[4:0]: Device ID

The ID[4:0] bits hold a device ID in the TDMCA mode.

8 Application and Implementation

NOTE

Information in the following applications sections is not part of the TI component specification, and TI does not warrant its accuracy or completeness. TI's customers are responsible for determining suitability of components for their purposes. Customers should validate and test their design implementation to confirm system functionality.

8.1 Application Information

The PCM1795 device is a software-controlled, differential current output DAC that can accept multiple formats of 16-, 24-, or 32-bit PCM audio data, DSD audio data, or TDMCA data. Because the PCM1795 is a current output part, in most cases a current to voltage stage is required before the signal is passed to the amplifier stage. A microcontroller or DSP can use SPI or I^2C to control the PCM1795 with ZEROL and ZEROR as status pins for the outputs. The PCM1795 requires a 5-V analog supply, as well as a 3.3-V digital supply.

8.2 Typical Applications

8.2.1 Typical Connection Diagram in PCM Mode

Figure 52 shows a typical application circuit for PCM mode operation.

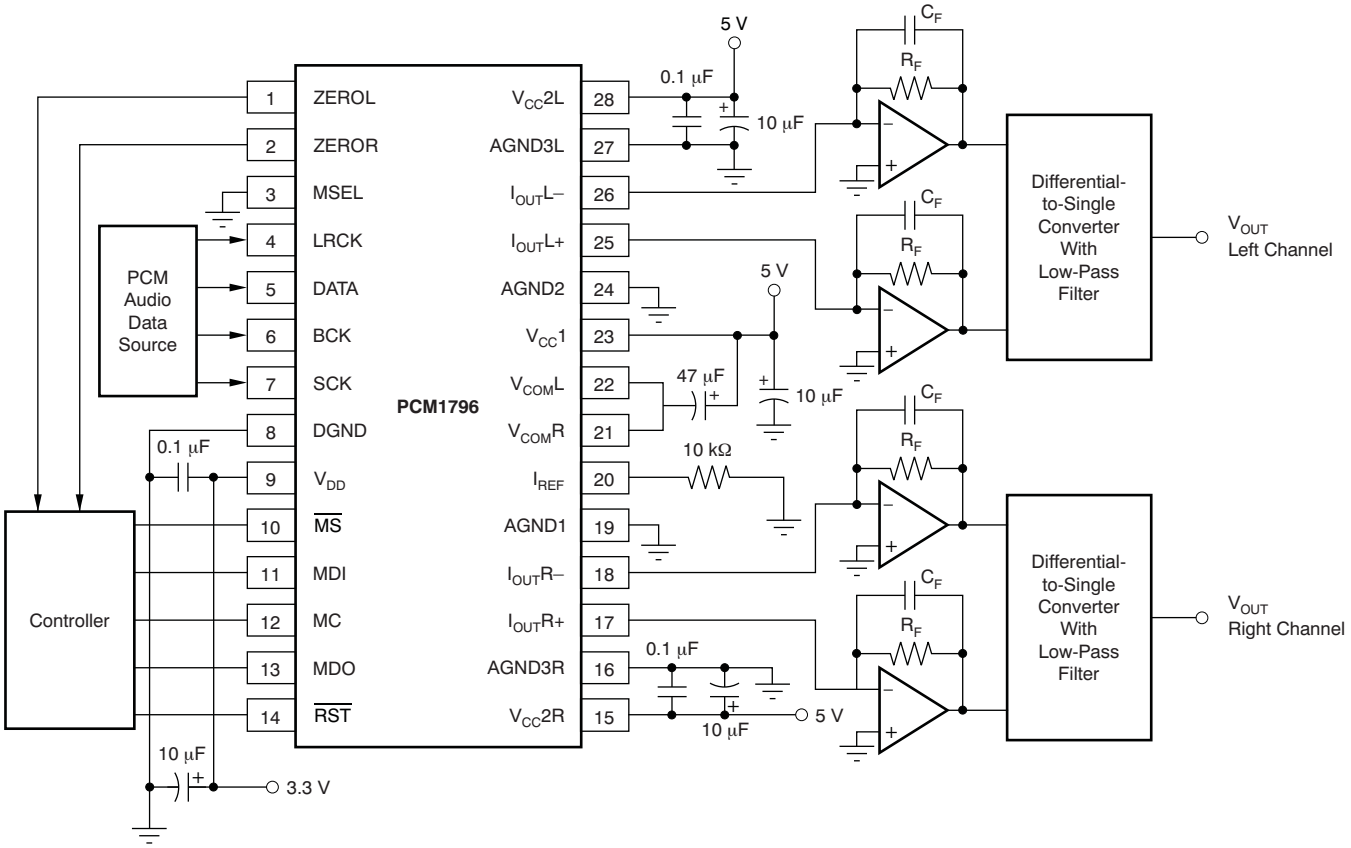


Figure 52. Typical Application Circuit for Standard PCM Audio Operation

8.2.1.1 Design Requirements

- Control: Host controller with SPI communication
- Audio Output: I/V output circuitry
- Audio Input: PCM, DSD, or TDMCA Digital Audio signal

Typical Applications (continued)

8.2.1.2 Detailed Design Procedure

The design of the application circuit is very important in order to actually realize the high S/N ratio of which the PCM1795 device is capable, because noise and distortion that are generated in an application circuit are not negligible.

In the third-order, low-pass filter (LPF) circuit of Figure 53, the output level of 2.1 V RMS and 123-dB signal-to-noise ratio is achieved.

Figure 54 shows a circuit for the DSD mode, which is a fourth-order LPF in order to reduce the out-of-band noise.

8.2.1.2.1 I/V Section

The current of the PCM1795 device on each of the output pins ($I_{OUT}L+$, $I_{OUT}L–$, $I_{OUT}R+$, $I_{OUT}R–$) is 4 mA_{PP} at 0 dB (full-scale). The voltage output level of the current-to-voltage (I/V) converter, V_I, is given by Equation 2.

$$V_I = 4\ mA_{PP} \times R_F \quad (2)$$

where

- R_F = feedback resistance of the I/V converter

An NE5534 operational amplifier is recommended for the I/V circuit to obtain the specified performance. Dynamic performance such as the gain bandwidth, settling time, and slew rate of the operational amplifier affects the audio dynamic performance of the I/V section.

8.2.1.2.2 Differential Section

The PCM1795 device voltage outputs are followed by differential amplifier stages that sum the differential signals for each channel, creating a single-ended I/V op-amp output. In addition, the differential amplifiers provide a low-pass filter function.

The operational amplifier recommended for the differential circuit is the low-noise type.

Typical Applications (continued)

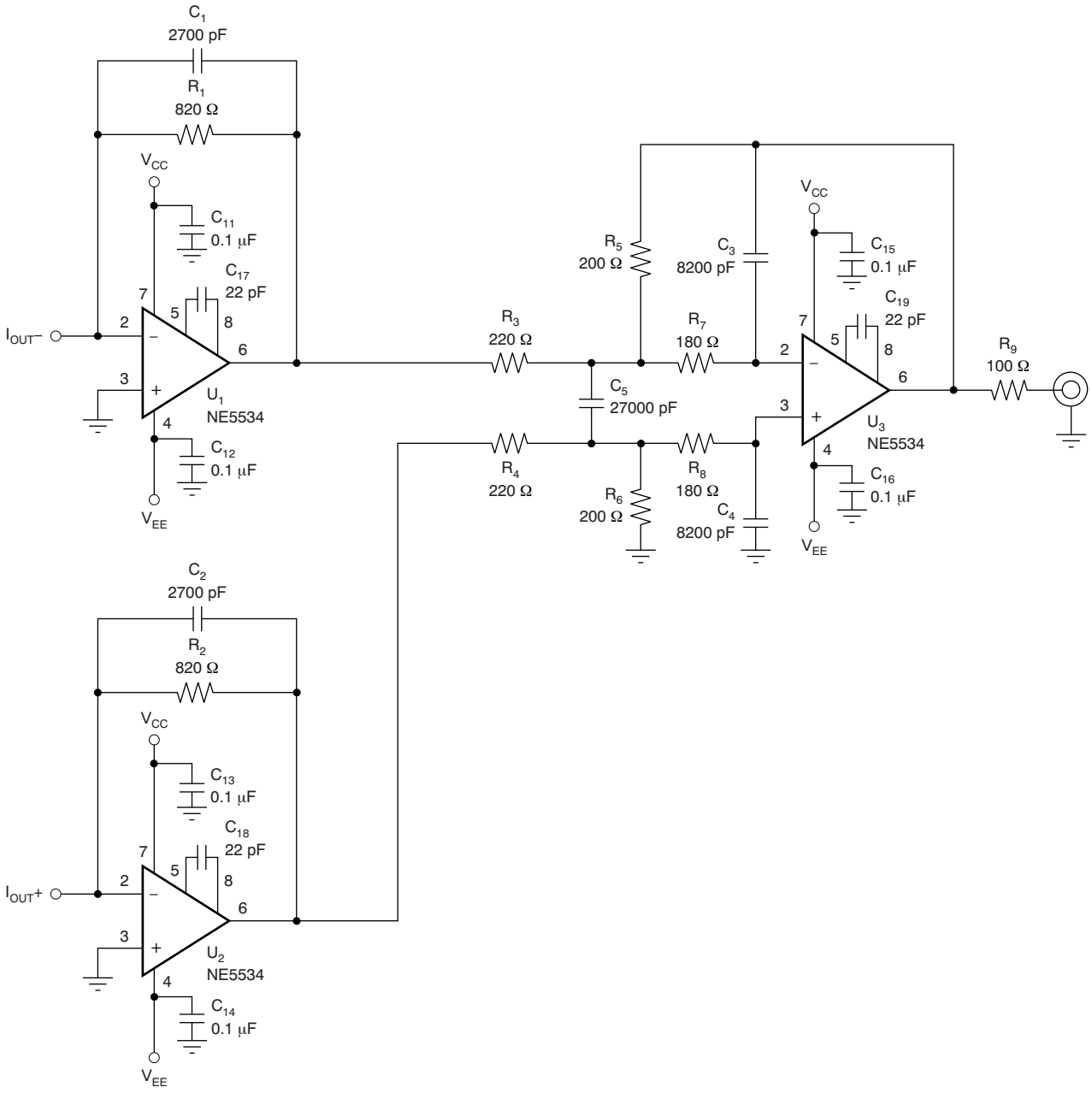


Figure 53. Measurement Circuit for PCM

Typical Applications (continued)

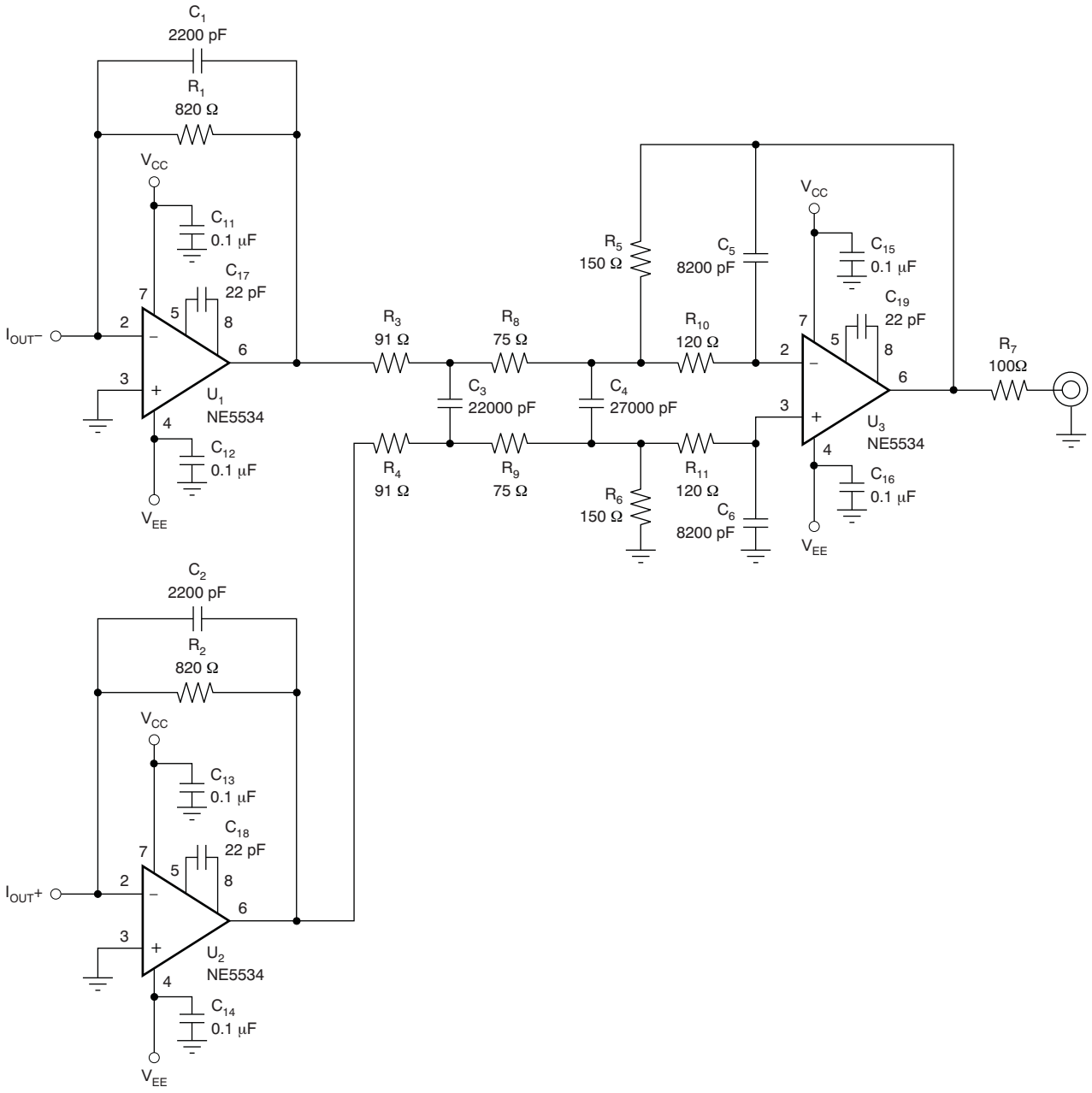
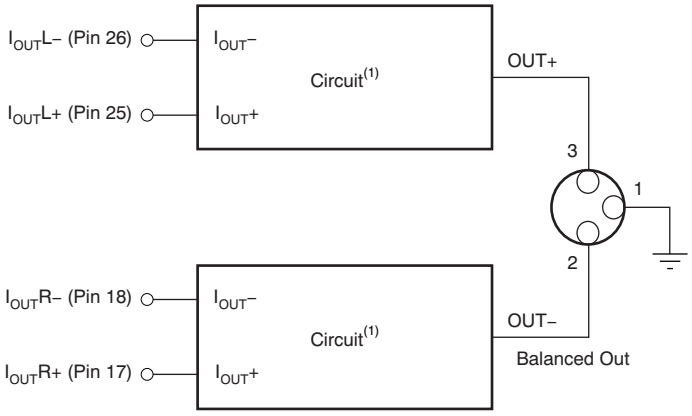


Figure 54. Measurement Circuit for DSD

Typical Applications (continued)



(1) Circuit corresponds to Figure 53.

Figure 55. Measurement Circuit for Monaural Mode

8.2.1.3 Application Curves

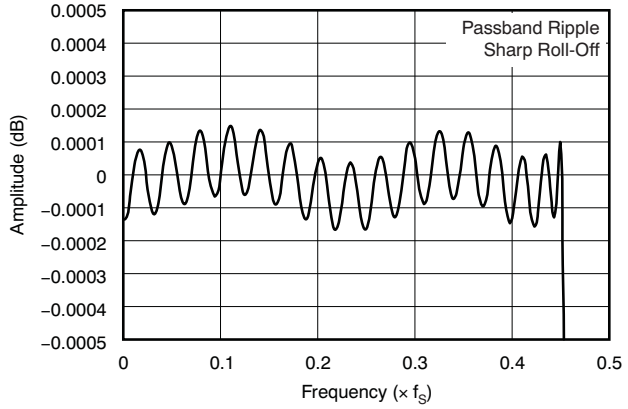


Figure 56. Amplitude vs Frequency

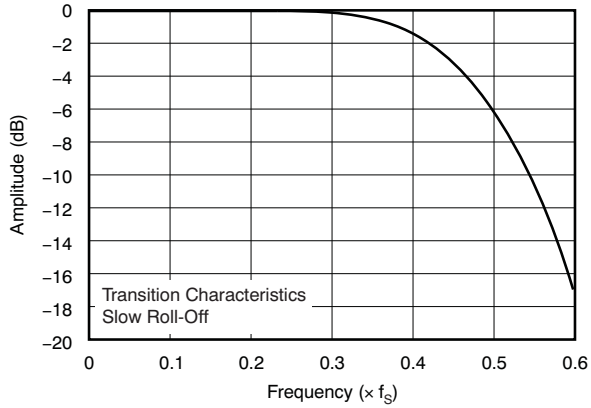


Figure 57. Amplitude vs Frequency

Typical Applications (continued)

8.2.2 Application for External Digital Filter Interface

Figure 58 shows the connection diagram for an external digital filter.

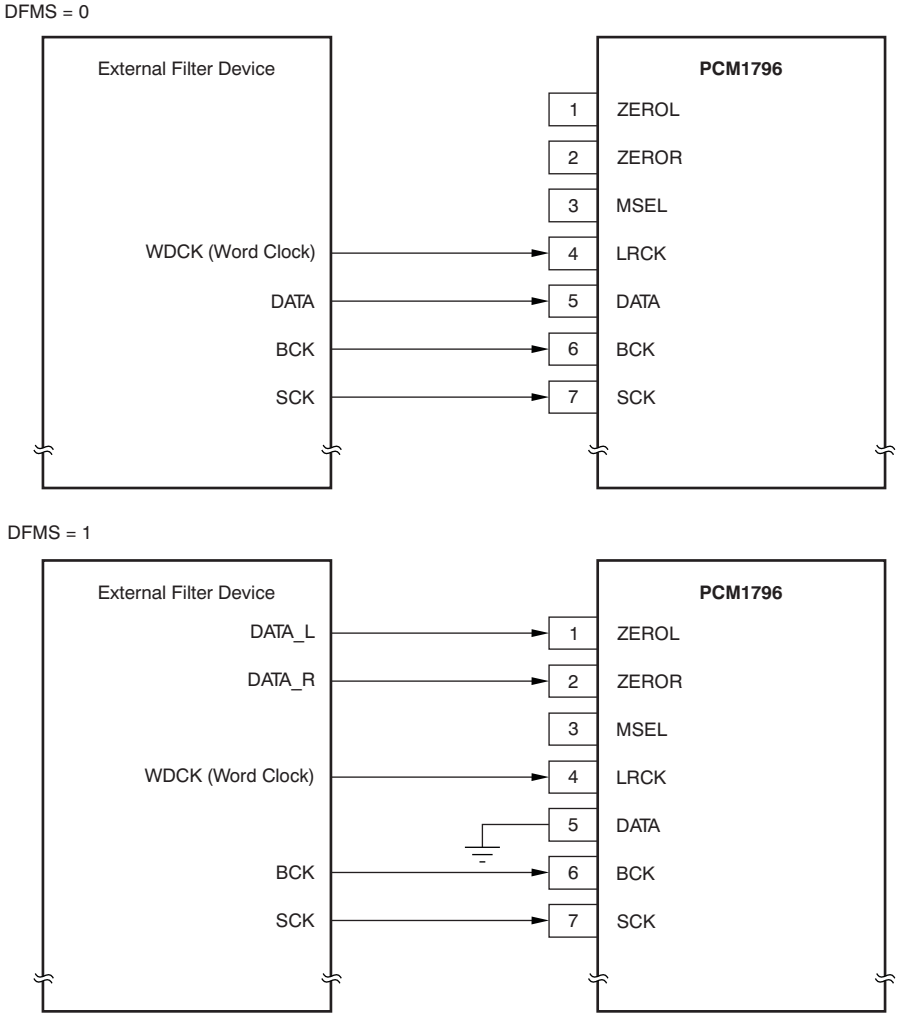


Figure 58. Connection Diagram for External Digital Filter (Internal DF Bypass Mode) Application

8.2.2.1 Design Requirements

- Control: Host controller with SPI communication
- Audio Output: I/V output circuitry
- Audio Input: Digital Audio Filter with I2S or DSD output

8.2.2.2 Detailed Design Procedure

8.2.2.2.1 Application for Interfacing With an External Digital Filter

For some applications, it may be desirable to use an external digital filter to perform the interpolation function, as it can provide improved stop-band attenuation when compared to the internal digital filter of the PCM1795 device.

The PCM1795 device supports several external digital filters, including:

- Texas Instruments DF1704 and DF1706
- Pacific Microsonics PMD200 HDCD filter/decoder IC
- Programmable DSPs

Typical Applications (continued)

The external digital filter application mode is accessed by programming the following bits in the corresponding control register:

- DFTH = 1 (register 20)

The pins used to provide the serial interface for the external digital filter are illustrated in Figure 58. The word clock (WDCK) signal must be operated at 8 times or 4 times the desired sampling frequency, f_S.

8.2.2.2.2 Pin Assignment When Using the External Digital Filter Interface

- LRCK (pin 4): WDCK as word clock input
- BCK (pin 6): Bit clock for audio data
- DATA (pin 5): Monaural audio data input when the DFMS bit is not set to 1
- ZEROL (pin 1): DATAL as left channel audio data input when the DFMS bit is set to 1
- ZEROR (pin 2): DATAR as right channel audio data input when the DFMS bit is set to 1

8.2.2.2.3 Audio Format

The PCM1795 device in the external digital filter interface mode supports right-justified audio formats including 16-bit, 24-bit, and 32-bit audio data, as shown in Figure 59. The audio format is selected by the FMT[2:0] bits of control register 18.

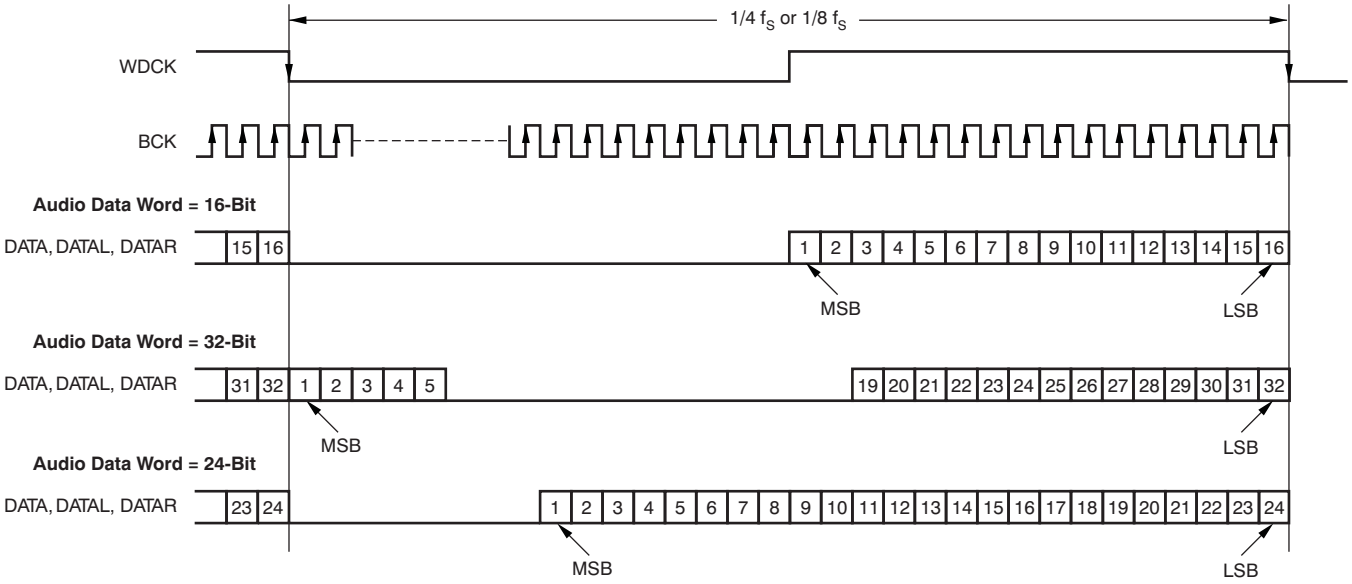


Figure 59. Audio Data Input Format for External Digital Filter (Internal DF Bypass Mode) Application

8.2.2.2.4 System Clock (SCK) and Interface Timing

The PCM1795 device in an application using an external digital filter requires the synchronization of WDCK and the system clock. The system clock is phase-free with respect to WDCK. Interface timing among WDCK, BCK, DATA, DATAL, and DATAR is shown in Figure 60 and Table 32.

Typical Applications (continued)

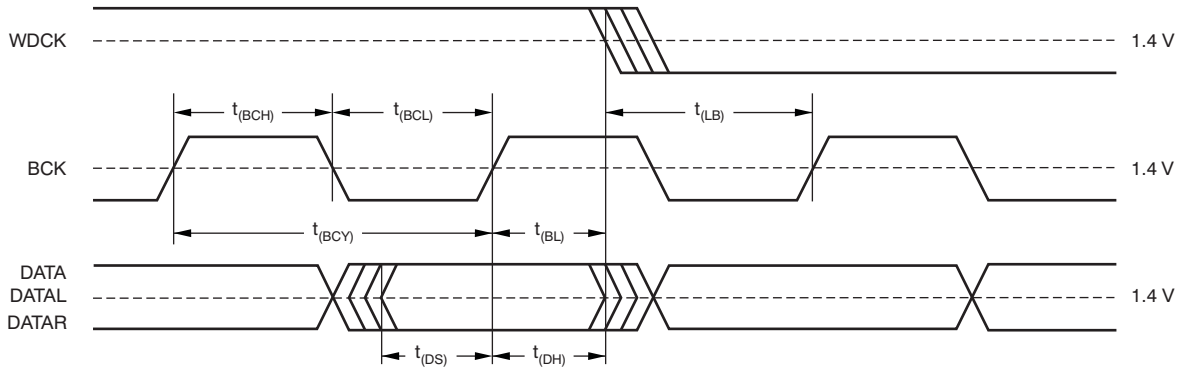


Figure 60. Audio Interface Timing for External Digital Filter (Internal DF Bypass Mode) Application

Table 32. Timing Characteristics for Figure 60

		MIN	MAX	UNIT
$t_{(BCY)}$	BCK pulse cycle time	20		ns
$t_{(BCL)}$	BCK pulse duration, low	7		ns
$t_{(BCH)}$	BCK pulse duration, high	7		ns
$t_{(BL)}$	BCK rising edge to WDCK falling edge	5		ns
$t_{(LB)}$	WDCK falling edge to BCK rising edge	5		ns
$t_{(DS)}$	DATA, DATAL, DATAR setup time	5		ns
$t_{(DH)}$	DATA, DATAL, DATAR hold time	5		ns

8.2.2.2.5 Functions Available in the External Digital Filter Mode

The external digital filter mode is selected by setting DSD = 0 (register 20, B5) and DFTH = 1 (register 20, B4).

The external digital filter mode allows access to the majority of the PCM1795 mode control functions.

Table 33 shows the register mapping available when the external digital filter mode is selected, along with descriptions of functions that are modified when using this mode selection.

Table 33. External Digital Filter Register Map

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	R/$\overline{W}$	0	0	1	0	0	0	0	X(1)	X	X	X	X	X	X	X
Register 17	R/$\overline{W}$	0	0	1	0	0	0	1	X	X	X	X	X	X	X	X
Register 18	R/$\overline{W}$	0	0	1	0	0	1	0	X	FMT2	FMT1	FMT0	X	X	X	X
Register 19	R/$\overline{W}$	0	0	1	0	0	1	1	REV	X	X	OPE	X	DFMS	X	INZD
Register 20	R/$\overline{W}$	0	0	1	0	1	0	0	X	SRST	0	1	MONO	CHSL	OS1	OS0
Register 21	R/$\overline{W}$	0	0	1	0	1	0	1	X	X	X	X	X	X	X	PCMZ
Register 22	R	0	0	1	0	1	1	0	X	X	X	X	X	X	ZFGR	ZFGL

(1) Function is disabled. No operation even if data bit is set.

8.2.2.2.5.1 FMT[2:0]: Audio Data Format Selection

Default value: 000

Table 34. FMT[2:0]

FMT[2:0]	AUDIO DATA FORMAT SELECTION
000	16-bit right-justified format
001	32-bit right-justified format
010	24-bit right-justified format (default)
Other	N/A

8.2.2.2.5.2 OS[1:0]: ΔΣ Modulator Oversampling Rate Selection

Default value: 00

Table 35. OS[1:0]

OS[1:0]	OPERATION SPEED SELECTION
00	8 times WDCK (default)
01	4 times WDCK
10	16 times WDCK
11	Reserved

The effective oversampling rate is determined by the oversampling performed by both the external digital filter and the ΔΣ modulator. For example, if the external digital filter is 8× oversampling, and OS[1:0] = 00 is selected, then the ΔΣ modulator oversamples by 8×, resulting in an effective oversampling rate of 64×. The 16× WDCK oversampling rate is not available above a 100-kHz sampling rate. If the oversampling rate selected is 16× WDCK, the system clock frequency must be over 256 f_S.

8.2.2.3 Application Curves

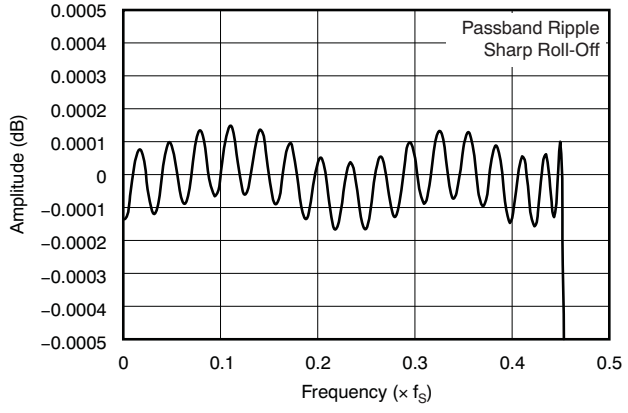


Figure 61. Amplitude vs Frequency

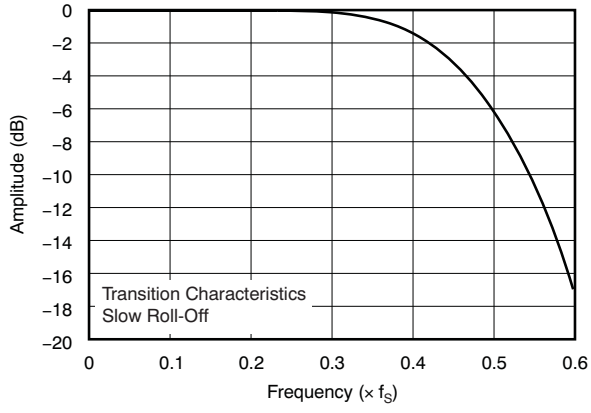


Figure 62. Amplitude vs Frequency

8.2.3 Application for DSD Format (DSD Mode) Interface

Figure 63 shows a connection diagram for DSD mode.

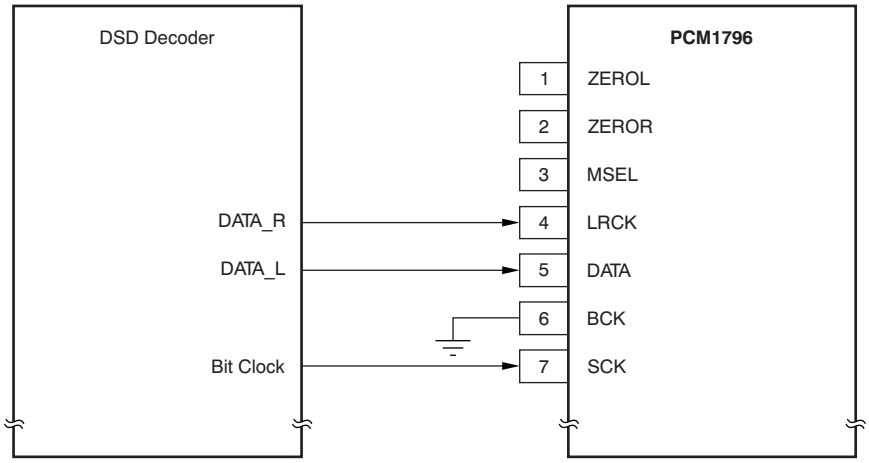


Figure 63. Connection Diagram in DSD Mode

8.2.3.1 Design Requirements

- Control: Host controller with SPI communication
- Audio Output: I/V output circuitry
- Audio Input: DSD Digital Audio input

8.2.3.2 Detailed Design Procedure

8.2.3.2.1 Features

This mode is used for interfacing directly to a DSD decoder, which is found in Super Audio CD™ (SACD) applications.

The DSD mode is accessed by programming the following bit in the corresponding control register.

- DSD = 1 (register 20)

The DSD mode provides a low-pass filtering function. The filtering is provided using an analog FIR filter structure. Four FIR responses are available and are selected by the DMF[1:0] bits of control register 18.

The DSD bit must be set before inputting DSD data; otherwise, the PCM1795 erroneously detects the TDMCA mode and commands are not accepted through the serial control interface.

8.2.3.2.2 Pin Assignment When Using DSD Format Interface

Several pins are redefined for DSD mode operation. These include:

- DATA (pin 5): DSDL as left-channel DSD data input
- LRCK (pin 4): DSDR as right-channel DSD data input
- SCK (pin 7): DBCK as bit clock for DSD data
- BCK (pin 6): Set low (N/A)

8.2.3.2.3 Requirements for System Clock

For operation in DSD mode, the bit clock (DBCK) is required on pin 7 of the PCM1795. The frequency of the bit clock can be *N* times the sampling frequency. Generally, *N* is 64 in DSD applications.

The interface timing between the bit clock and DSDL and DSDR is required to meet the setup and hold time specifications shown in Figure 65 and Table 36.

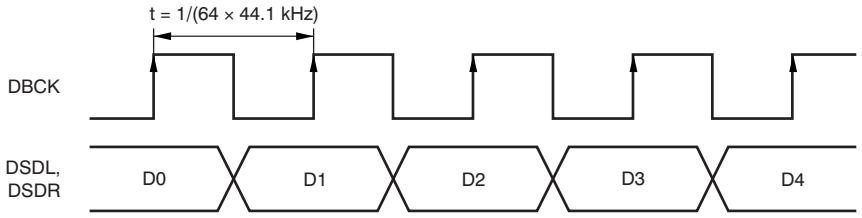


Figure 64. Normal Data Output Form From DSD Decoder

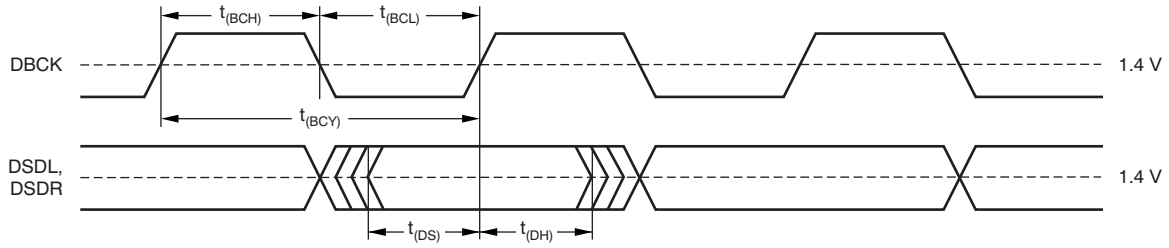


Figure 65. Timing for DSD Audio Interface

Table 36. Timing Characteristics for Figure 65

		MIN	MAX	UNIT
$t_{(BCY)}$	DBCK pulse cycle time	85 (1)		ns
$t_{(BCH)}$	DBCK high-level time	30		ns
$t_{(BCL)}$	DBCK low-level time	30		ns
$t_{(DS)}$	DSDL, DSDR setup time	10		ns
$t_{(DH)}$	DSDL, DSDR hold time	10		ns

(1) 2.8224 MHz × 4. (2.8224 MHz = 64 × 44.1 kHz. This value is specified as a sampling rate of DSD.

8.2.3.2.4 DSD Mode Configuration and Function Controls

8.2.3.2.4.1 Configuration for the DSD Interface Mode

The DSD interface mode is selected by setting DSD = 1 (register 20, B5).

Table 37. DSD Mode Register Map

REGISTER	B15	B14	B13	B12	B11	B10	B9	B8	B7	B6	B5	B4	B3	B2	B1	B0
Register 16	R/$\overline{W}$	0	0	1	0	0	0	0	X (1)	X	X	X	X	X	X	X
Register 17	R/$\overline{W}$	0	0	1	0	0	0	1	X	X	X	X	X	X	X	X
Register 18	R/$\overline{W}$	0	0	1	0	0	1	0	X	X	X	X	DMF1	DMF0	X	X
Register 19	R/$\overline{W}$	0	0	1	0	0	1	1	REV	X	X	OPE	X	X	X	X
Register 20	R/$\overline{W}$	0	0	1	0	1	0	0	X	SRST	1	X	MONO	CHSL	OS1	OS0
Register 21	R	0	0	1	0	1	0	1	X	X	X	X	X	DZ1	DZ0	X
Register 22	R	0	0	1	0	1	1	0	X	X	X	X	X	X	ZFGR	ZFGL

(1) Function is disabled. No operation even if data bit is set.

8.2.3.2.4.2 DMF[1:0]: Analog-FIR Performance Selection

Default value: 00

Table 38. DMF[1:0]

DMF[1:0]	ANALOG-FIR PERFORMANCE SELECTION
00	FIR-1 (default)
01	FIR-2
10	FIR-3
11	FIR-4

Plots for the four analog finite impulse response (FIR) filter responses are shown in *Analog FIR Filter Performance in DSD Mode* .

8.2.3.2.4.3 OS[1:0]: Analog-FIR Operation-Speed Selection

Default value: 00

Table 39. OS[1:0]

OS[1:0]	OPERATING SPEED SELECTION
00	f_{DBCK} (default)
01	$f_{DBCK}/2$
10	Reserved
11	$f_{DBCK}/4$

The OS bit in the DSD mode is used to select the operating rate of the analog FIR. The OS bits must be set before setting the DSD bit to '1'.

8.2.3.3 Application Curves

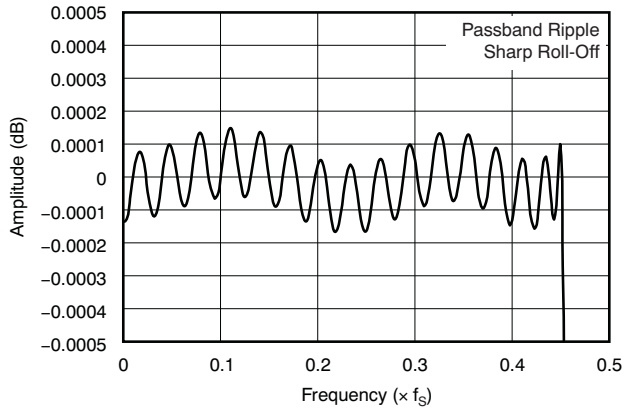


Figure 66. Amplitude vs Frequency

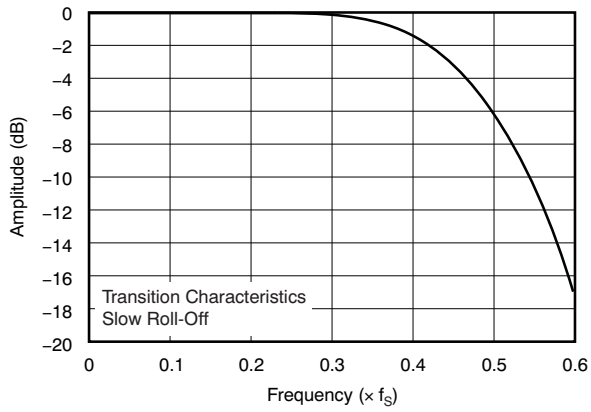


Figure 67. Amplitude vs Frequency

8.2.4 TDMCA Interface Format

The PCM1795 device supports the time-division-multiplexed command and audio (TDMCA) data format to simplify the host control serial interface. TDMCA format is designed not only for the multichannel buffered serial port description (McBSP) of TI DSPs but also for any programmable devices. TDMCA format can transfer not only audio data but also command data, so that it can be used together with any kind of device that supports TDMCA format. The TDMCA frame consists of a command field, extended command field, and some audio data fields. Those audio data are transported to IN devices (such as a DAC) and/or from OUT devices (such as an ADC). The PCM1795 is an IN device. LRCK and BCK are used with both IN and OUT devices so that the sample frequency of all devices in a system must be the same. The TDMCA mode supports a maximum of 30 device IDs. The maximum number of audio channels depends on the BCK frequency.

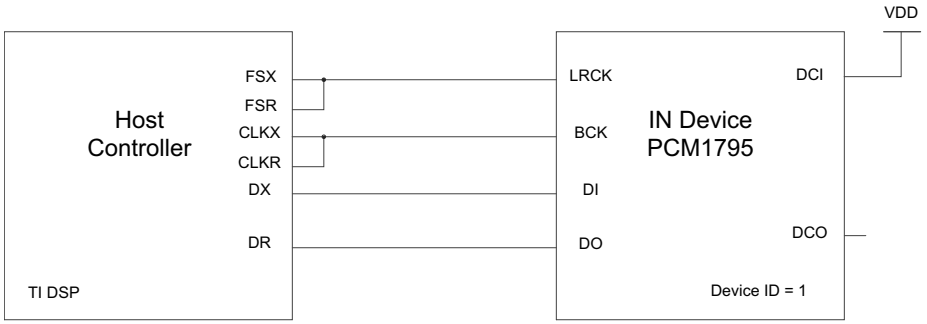


Figure 68. TDMCA Diagram

8.2.4.1 Design Requirements

- Control: TDMCA control information
- Audio Input: TDMCA input with LRCK signal with a pulse of two BCK clocks
- Audio Output: I/V output circuitry

8.2.4.2 Detailed Design Procedure

8.2.4.2.1 TDMCA Mode Determination

The PCM1795 device recognizes the TDMCA mode automatically when it receives an LRCK signal with a pulse duration of two BCK clocks. If the TDMCA mode operation is not needed, the duty cycle of LRCK must be 50%. Figure 69 shows the LRCK and BCK timing that determines the TDMCA mode. The PCM1795 device enters TDMCA mode after two continuous TDMCA frames. Any TDMCA commands can be issued during the next TDMCA frame after entering TDMCA mode.

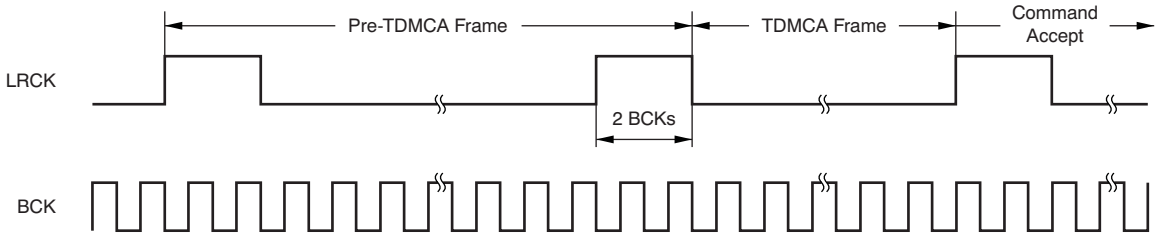


Figure 69. LRCK and BCK Timing for Determination of TDMCA Mode

8.2.4.2.2 TDMCA Terminals

TDMCA requires six signals: four signals are for the command and audio data interface, and one pair for daisy-chaining. These signals can be shared as shown in Table 40. The DO signal has a 3-state output so that it can be connected directly to other devices.

Table 40. TDMCA Terminals

TERMINAL NAME	TDMCA NAME	PROPERTY	DESCRIPTION
LRCK	LRCK	Input	TDMCA frame start signal; it must be the same as the sampling frequency
BCK	BCK	Input	TDMCA clock; its frequency must be high enough to communicate a TDMCA frame within an LRCK cycle
DATA	DI	Input	TDMCA command and audio data input signal
MDO	DO	Output	TDMCA command data 3-state output signal
MC	DCI	Input	TDMCA daisy-chain input signal
$\overline{MS}$	DCO	Output	TDMCA daisy-chain output signal

8.2.4.2.3 Device ID Determination

TDMCA mode also supports a multichip implementation in one system. This capability means that a host controller (DSP) can simultaneously support several TDMCA devices, which can be of the same type or different types, including PCM devices. The PCM devices are categorized as either IN devices, OUT devices, IN/OUT devices, and NO devices. The IN device has an input port to receive audio data; the OUT device has an output port to supply audio data; the IN/OUT device has both input and output ports for audio data; and the NO device has no port for audio data, but requires command data from the host. A DAC is an IN device; an ADC is an OUT device; a codec is an IN/OUT device; and a PLL is a NO device. The PCM1795 is an IN device. For the host controller to distinguish the devices, each device is assigned its own device ID by the daisy-chain. The devices obtain their own device IDs automatically by connecting the DCI to the DCO of the preceding device and the DCO to the DCI of the following device in the daisy-chain. The daisy-chains are categorized as the IN chain and the OUT chain, which are completely independent and equivalent. Figure 70 shows an example daisy-chain connection. If a system must chain the PCM1795 device and a NO device in the same IN or OUT chain, the NO device must be chained at the back end of the chain because it does not require any audio data. Figure 71 shows an example TDMCA system including an IN chain and an OUT chain with a TI DSP. For a device to get its own device ID, the DID signal must be set to '1' (see the *Command Field* section for details), and LRCK and BCK must be driven in the TDMCA mode for all PCM devices that are chained. The device at the top of the chain knows its device ID is '1' because its DCI is fixed high. Other devices count the BCK pulses and observe the respective DCI signal to determine ID and position in the chain. Figure 72 shows the initialization of each device ID.

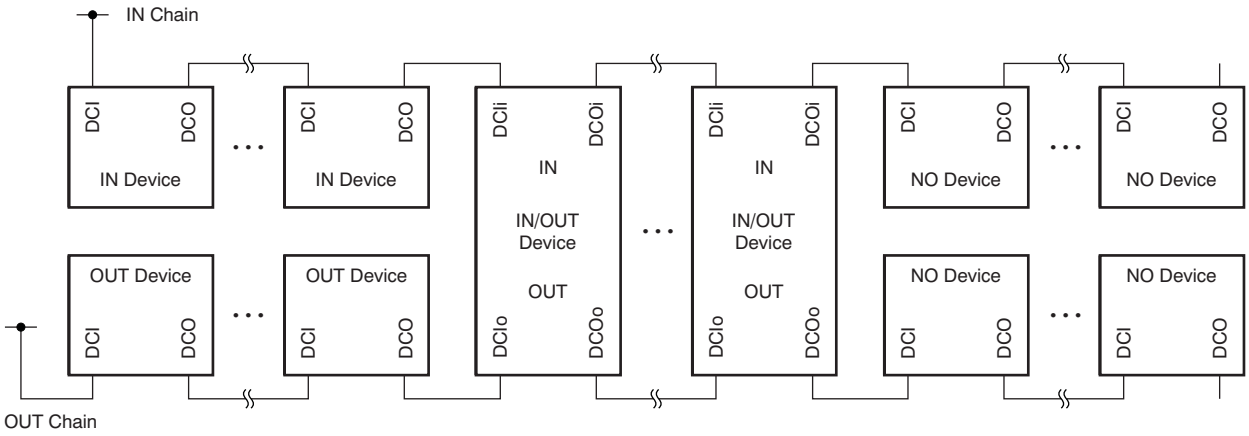


Figure 70. Daisy-Chain Connection Example

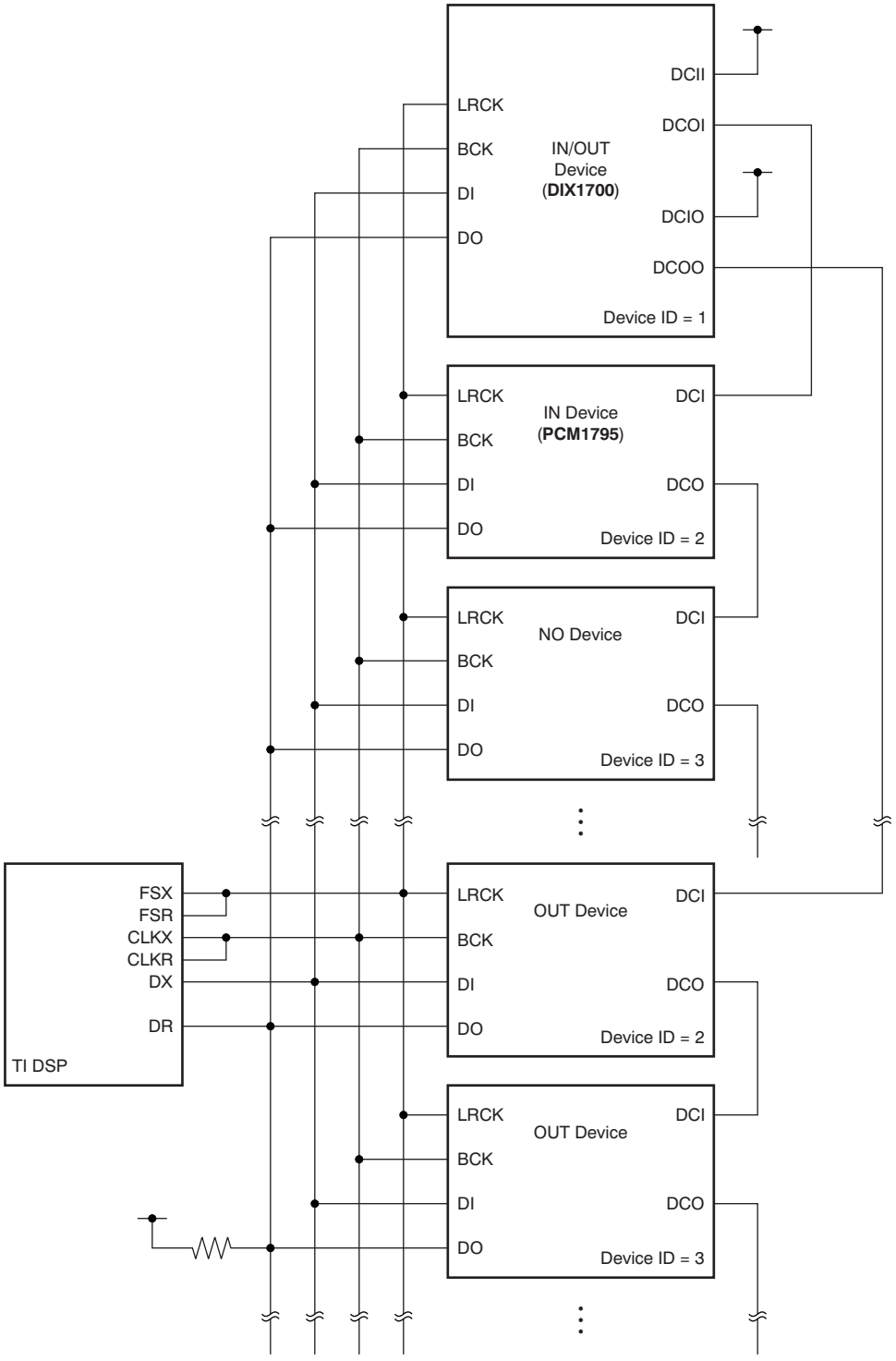


Figure 71. IN Daisy-Chain and OUT Daisy-Chain Connection Example for a Multichip System

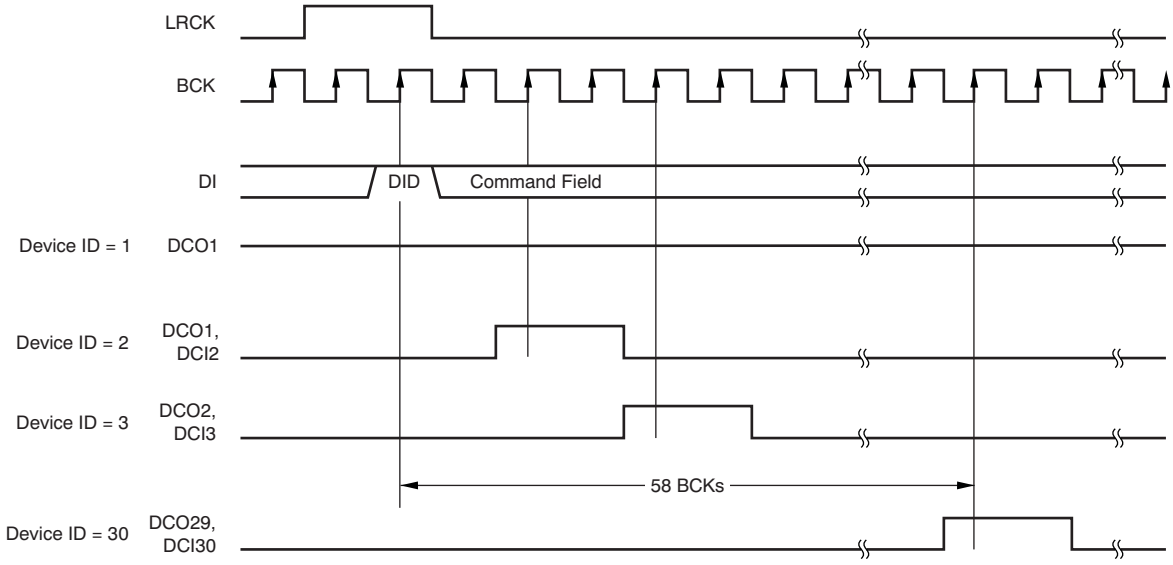


Figure 72. Device ID Determination Sequence

8.2.4.2.4 TDMCA Frame

In general, the TDMCA frame consists of the command field, extended command (EMD) field, and audio data fields. All fields are 32 bits long, but the lowest byte has no meaning. The MSB is transferred first for each field. The command field is always transferred as the first packet of the frame. The EMD field is transferred if the EMD flag of the command field is high. If any EMD packets are transferred, no audio data follow the EMD packets. This frame is for quick system initialization. All devices of a daisy-chain should respond to the command field and extended command field. The PCM1795 has two audio channels that can be selected by OPE (register 19). If the OPE bit is not set to high, those audio channels are transferred. Figure 73 shows the general TDMCA frame. If some DACs are enabled, but corresponding audio data packets are not transferred, the analog outputs are unpredictable.

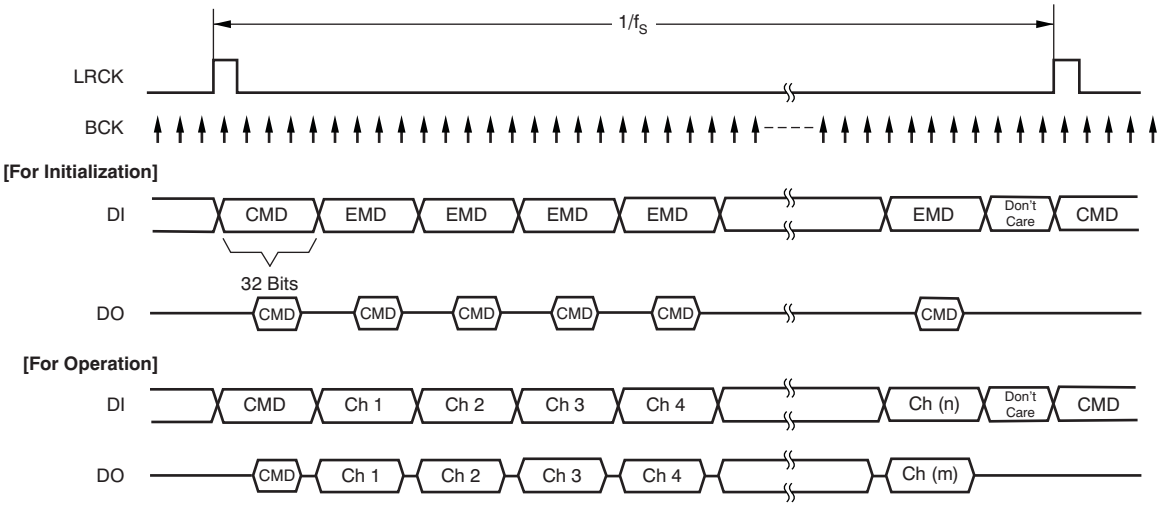


Figure 73. General TDMCA Frame

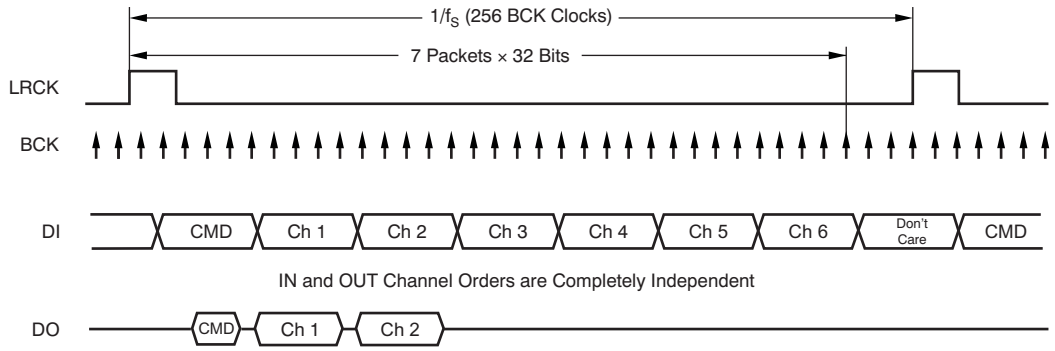


Figure 74. TDMCA Frame Example of Six-Channel DAC and Two-Channel ADC With Command Read

8.2.4.2.5 Command Field

The normal command field is defined as shown in Figure 75. When the DID bit (MSB) is '1', this frame is used only for device ID determination, and all remaining bits in the field are ignored.

Figure 75. Normal Command Field

8.2.4.2.5.1 Bit 31: Device ID Enable Flag

The PCM1795 operates to get its own device ID for TDMCA initialization if this bit is high.

8.2.4.2.5.2 Bit 30: Extended Command Enable Flag

The EMD packet is transferred if this bit is high; otherwise, it is skipped. Once this bit is high, this frame does not contain any audio data. This is for system initialization.

8.2.4.2.5.3 Bit 29: Daisy-Chain Selection Flag

A high setting designates OUT-chain devices, low designates IN-chain devices. The PCM1795 is an IN device, so the DCS bit must be set low.

8.2.4.2.5.4 Bits[28:24]: Device ID

The device ID is 5 bits long and it can be defined. These bits identify the order of a device in the IN or OUT daisy-chain. The top of the daisy-chain defines device ID 1 and successive devices are numbered 2, 3, 4, etc. All devices for which the DCI is fixed high are also defined as ID 1. The maximum device ID is 30 each in the IN and OUT chains. If a device ID of 0x1F is used, all devices are selected as broadcast when in the write mode. If a device ID of 0x00 is used, no device is selected.

8.2.4.2.5.5 Bit 23: Command Read/Write flag

If this bit is high, the command is a read operation.

8.2.4.2.5.6 Bits[22:16]: Register ID

The register ID is 7 bits long.

8.2.4.2.5.7 Bits[15:8]: Command data

The command data are 8 bits long. Any valid data can be chosen for each register.

8.2.4.2.5.8 Bits[7:0]: Not used

These bits are never transported when a read operation is performed.

8.2.4.2.6 Extended Command Field

The extended command field is the same as the command field, except that it does not have a DID flag. Figure 76 defines the extended command field.

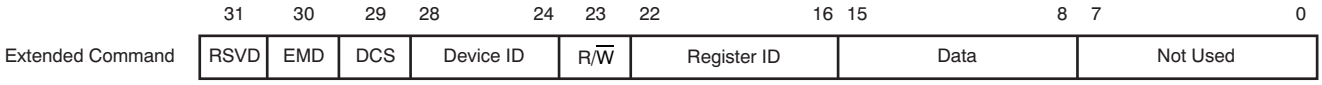


Figure 76. Extended Command Field

8.2.4.2.7 Audio Fields

The audio field is 32 bits long and the audio data are transferred MSB first, so the other fields must be filled with 0s as shown in Figure 77.

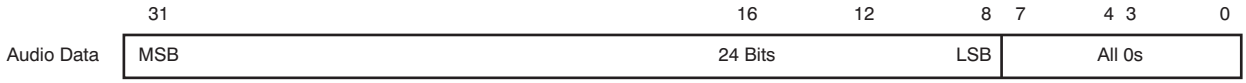


Figure 77. Audio Field Example

8.2.4.2.8 TDMCA Register Requirements

The TDMCA mode requires device ID and audio channel information, as previously described. The OPE bit in register 19 indicates audio channel availability and register 23 indicates the device ID. Register 23 is used only in the TDMCA mode; see the mode control register map of Table 10.

8.2.4.2.9 Register Write/Read Operation

The command supports register write and read operations. If the command requests to read one register, the read data are transferred on DO during the data phase of the timing cycle. The DI signal can be retrieved at the positive edge of BCK, and the DO signal is driven at the negative edge of BCK. DO is activated one BCK cycle early to compensate for the output delay caused by high impedance. Figure 78 shows the TDMCA write and read timing.

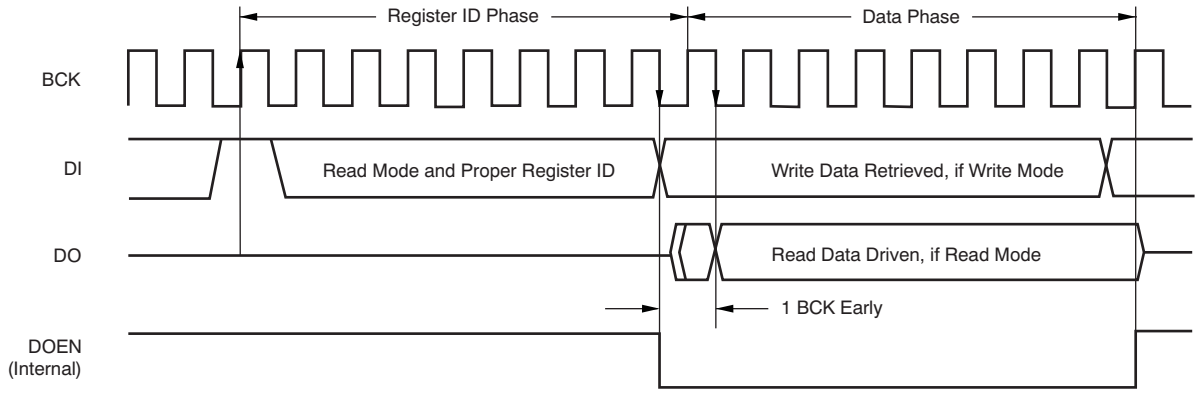


Figure 78. TDMCA Write and Read Operation Timing

8.2.4.2.10 TDMCA Mode Operation

DCO specifies the owner of the next audio channel in TDMCA mode operation. When a device retrieves its own audio channel data, DCO goes high during the last audio channel period. Figure 79 shows the DCO output timing in TDMCA mode operation. The host controller ignores the behavior of DCI and DCO. DCO indicates the last audio channel of each device. Therefore, DCI means the next audio channel is allocated.

If some devices are skipped because of no active audio channel, the skipped devices must notify the next device that the DCO will be passed through the next DCI. Figure 80 and Figure 81 show DCO timing with skip operation. Figure 82 and Table 41 show the ac timing of the daisy-chain signals.

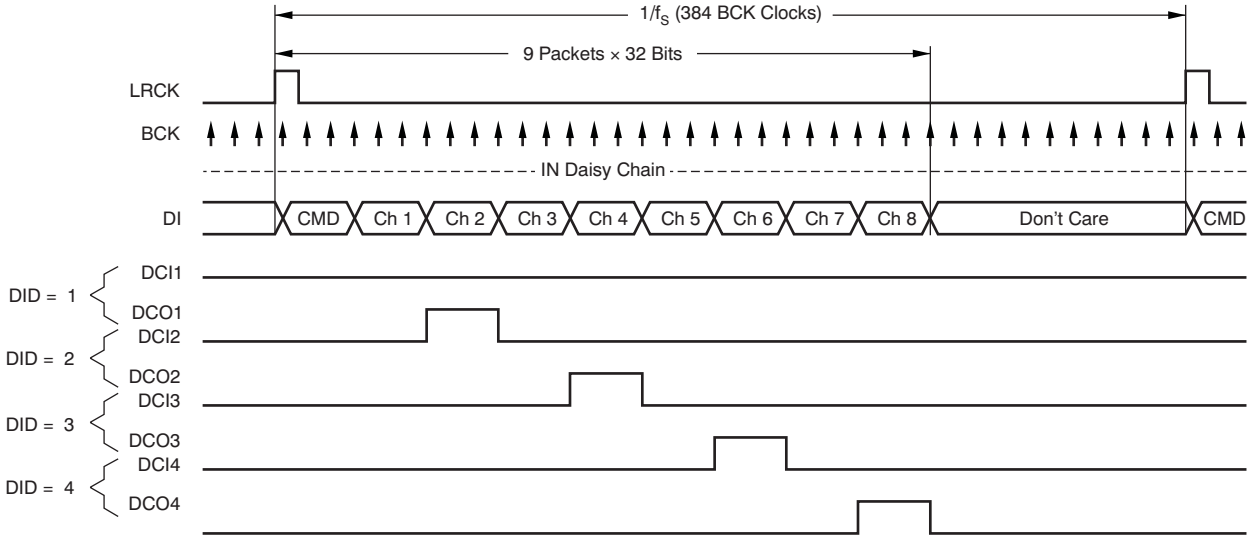


Figure 79. DCO Output Timing of TDMCA Mode Operation

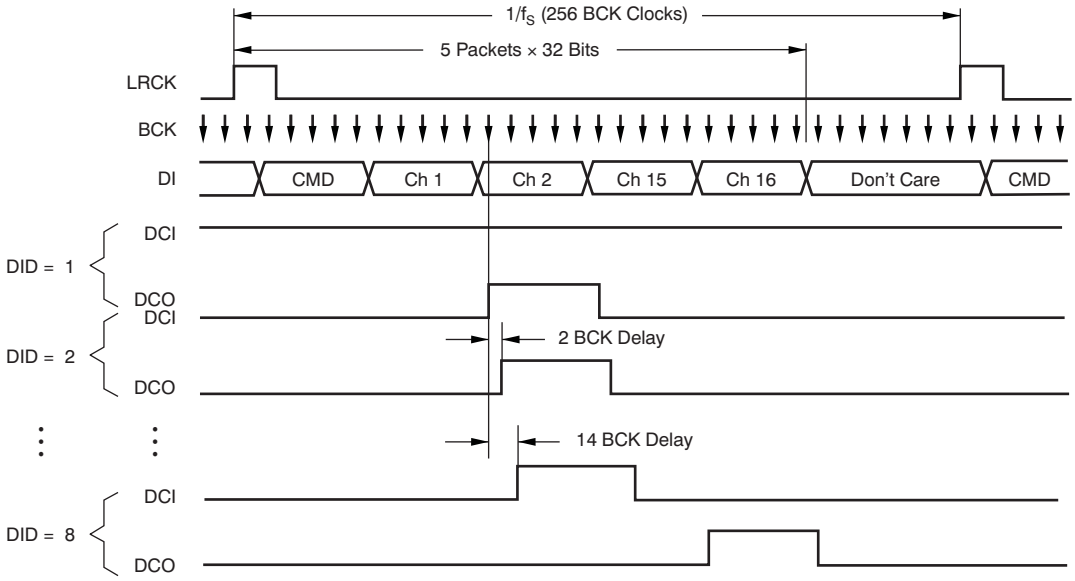


Figure 80. DCO Output Timing With Skip Operation

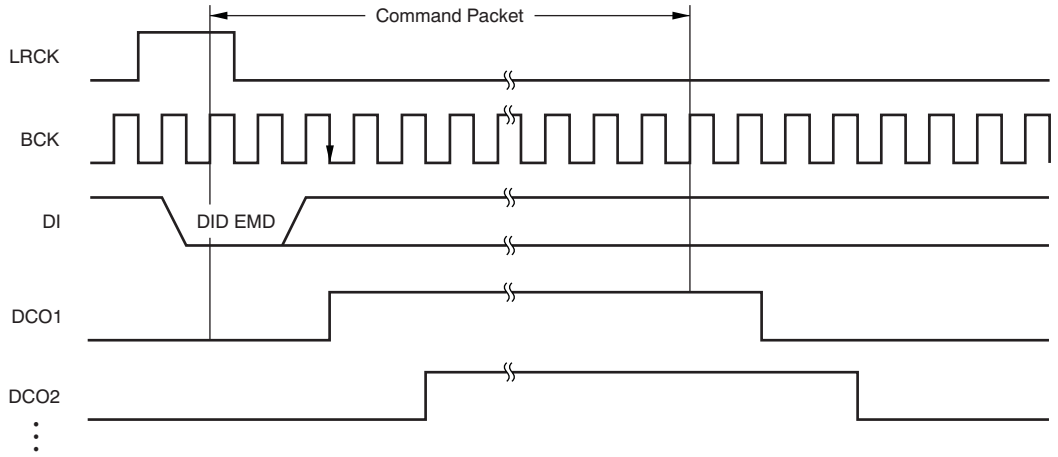


Figure 81. DCO Output Timing With Skip Operation (for Command Packet 1)

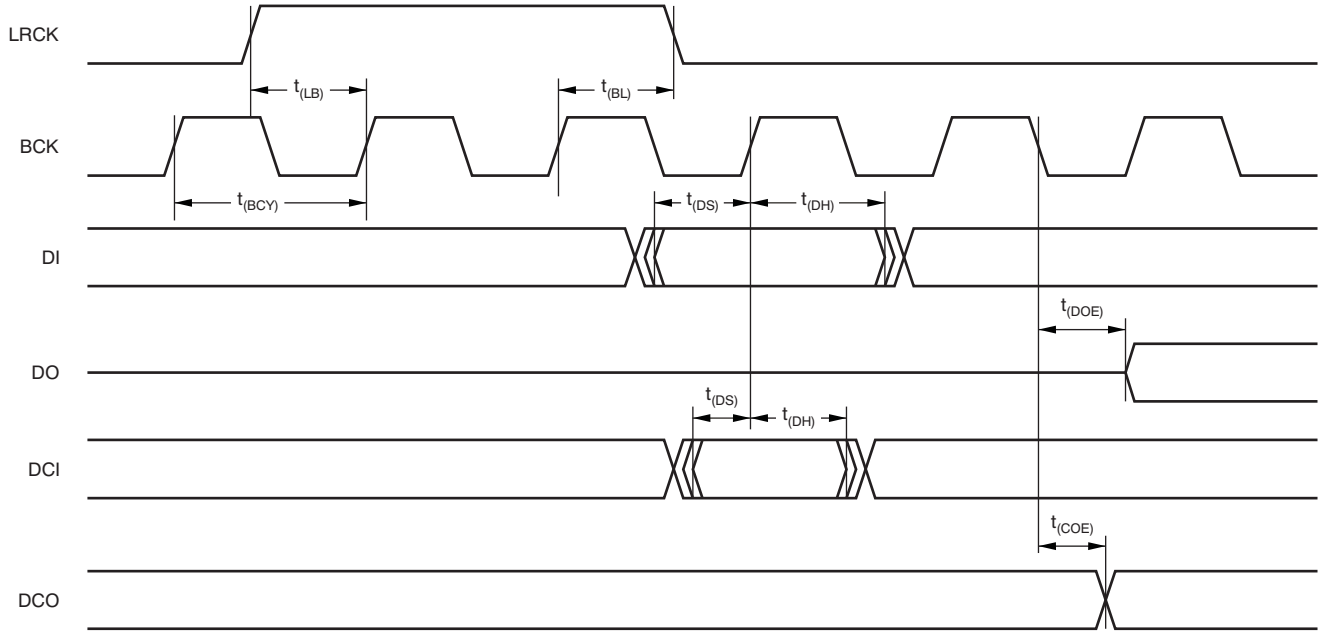


Figure 82. AC Timing of Daisy-Chain Signals

Table 41. Timing Characteristics for Figure 82

		MIN	MAX	UNIT
$t_{(BCY)}$	BCK pulse cycle time	20		ns
$t_{(LB)}$	LRCK setup time	0		ns
$t_{(BL)}$	LRCK hold time	3		ns
$t_{(DS)}$	DI setup time	0		ns
$t_{(DH)}$	DI hold time	3		ns
$t_{(DS)}$	DCI setup time	0		ns
$t_{(DH)}$	DCI hold time	3		ns
$t_{(DOE)}$	DO output delay(1)		8	ns
$t_{(COE)}$	DCO output delay(1)		6	ns

(1) Load capacitance is 10 pF.

9 Power Supply Recommendations

The PCM1795 device requires a 5-V nominal supply and a 3.3-V nominal supply. The 5-V supply is for the analog circuitry powered by V_{CC1}, V_{CC2L}, and V_{CC2R} pins. The 3.3-V supply is for the digital circuitry powered by the V_{DD} pin. The decoupling capacitors for the power supplies should be placed close to the device terminals.

10 Layout

10.1 Layout Guidelines

Designers should try to use the same ground between AGND and DGND to avoid any potential voltage difference between them. Ensure that the return currents for digital signals will avoid the AGND pin or the input signals to the I/V stage. Avoid running high-frequency clock and control signals near AGND, or any of the VOUT pins where possible. The pin layout of the PCM1795 device partitions into two sides, the analog side and the digital side. Providing the system is partitioned in such a way that digital signals are routed away from the analog sections, then no digital return currents (for example, clocks) should be generated in the analog circuitry.

- Decoupling capacitors should be placed as close to the V_{CC1}, V_{CC2L}, V_{CCR2}, V_{COML}, V_{COMR}, and V_{DD} pins as possible.
- Further guidelines can be found in Figure 83.

10.2 Layout Example

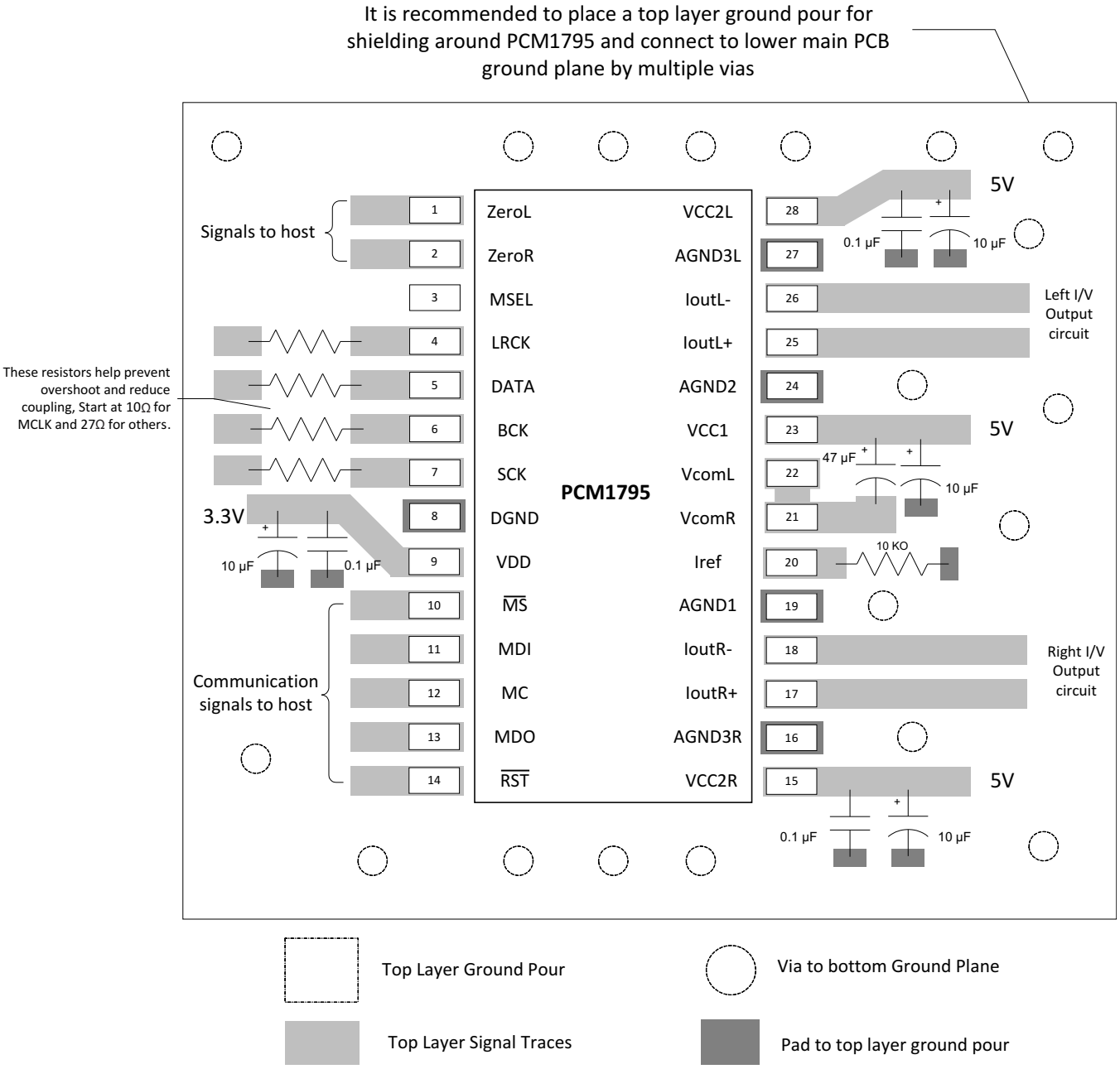


Figure 83. Layout Recommendation

11 Device and Documentation Support

11.1 Device Support

11.1.1 Third-Party Products Disclaimer

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11.3 Electrostatic Discharge Caution

These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

11.4 Glossary

SLYZ022 — *TI Glossary*.

This glossary lists and explains terms, acronyms, and definitions.

12 Mechanical, Packaging, and Orderable Information

The following pages include mechanical, packaging, and orderable information. This information is the most current data available for the designated devices. This data is subject to change without notice and revision of this document. For browser-based versions of this data sheet, refer to the left-hand navigation.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish (6)	MSL Peak Temp (3)	Op Temp (°C)	Device Marking (4/5)	Samples
PCM1795DB	ACTIVE	SSOP	DB	28	50	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1795	Samples
PCM1795DBR	ACTIVE	SSOP	DB	28	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-1-260C-UNLIM	-25 to 85	PCM1795	Samples

(1) The marketing status values are defined as follows:
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NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
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Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. - The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

(4) There may be additional marking, which relates to the logo, the lot trace code information, or the environmental category on the device.

(5) Multiple Device Markings will be inside parentheses. Only one Device Marking contained in parentheses and separated by a "~" will appear on a device. If a line is indented then it is a continuation of the previous line and the two combined represent the entire Device Marking for that device.

(6) Lead/Ball Finish - Orderable Devices may have multiple material finish options. Finish options are separated by a vertical ruled line. Lead/Ball Finish values may wrap to two lines if the finish value exceeds the maximum column width.

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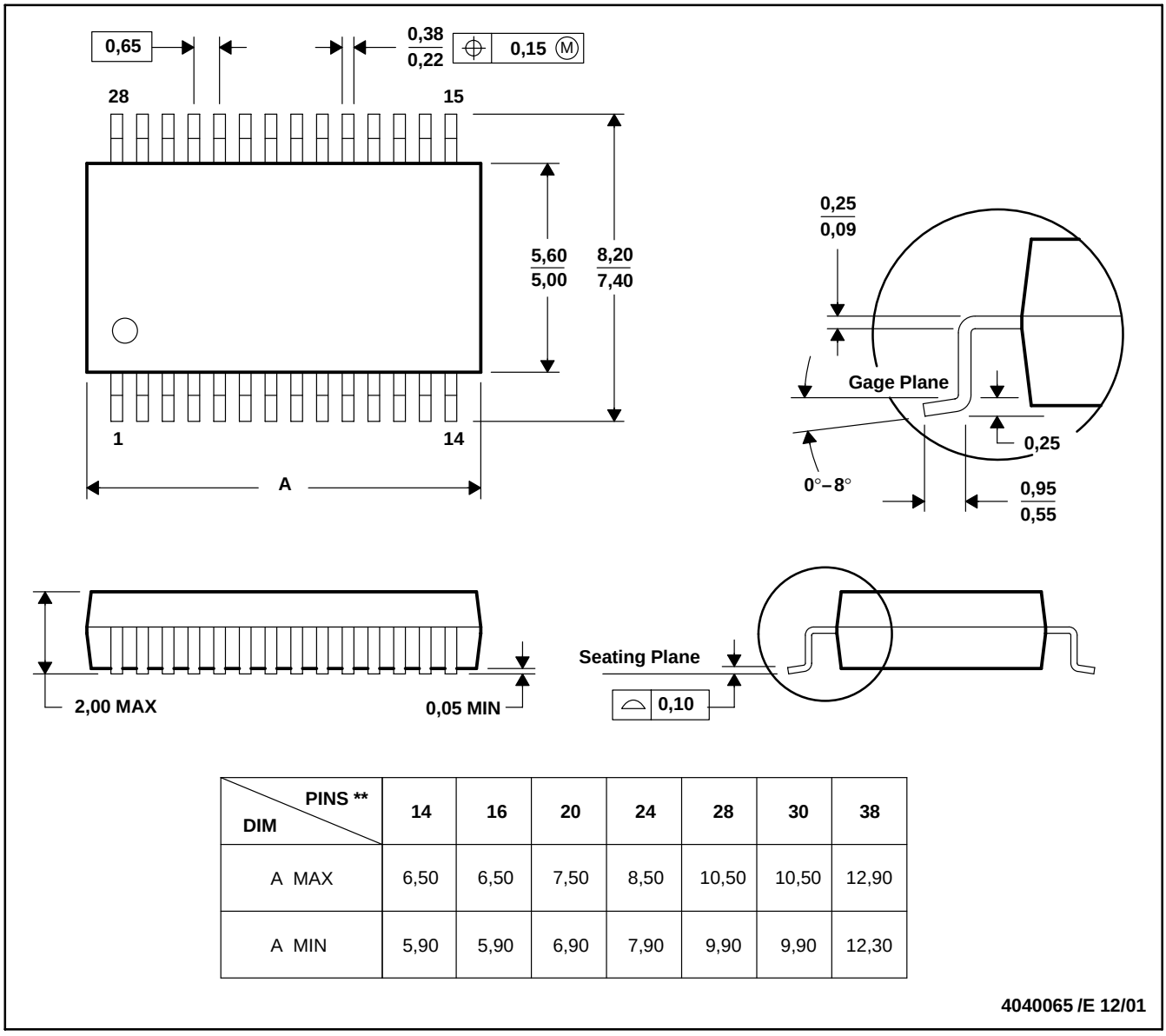
MSSO002E – JANUARY 1995 – REVISED DECEMBER 2001

DB (R-PDSO-G)** **PLASTIC SMALL-OUTLINE**

28 PINS SHOWN



DIM \ PINS **	14	16	20	24	28	30	38
A MAX	6,50	6,50	7,50	8,50	10,50	10,50	12,90
A MIN	5,90	5,90	6,90	7,90	9,90	9,90	12,30

4040065 /E 12/01

NOTES: A. All linear dimensions are in millimeters.
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion not to exceed 0,15.
D. Falls within JEDEC MO-150

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