LTM4602

6A High Efficiency DC/DC µModule

FEATURES

- **Complete Switch Mode Power Supply**
- **Wide Input Voltage Range: 4.5V to 20V**
- **6A DC, 8A Peak Output Current**
- **0.6V to 5V Output Voltage**
- **1.5% Output Voltage Regulation**
- **Ultrafast Transient Response**
- **Current Mode Control**
- **Pb-Free (e4) RoHS Compliant Package with Gold-Pad Finish**
- **Pin Compatible with the LTM4600**
- Up to 92% Efficiency
- Programmable Soft-Start
- Output Overvoltage Protection
- Optional Short-Circuit Shutdown Timer
- See the LTM4602HV for Operation Up to $28V_{IN}$
- Small Footprint, Low Profile (15mm × 15mm × 2.8mm) Surface Mount LGA Package

APPLICATIONS

- Telecom and Networking Equipment
- Servers
- Industrial Equipment
- Point of Load Regulation

DESCRIPTION

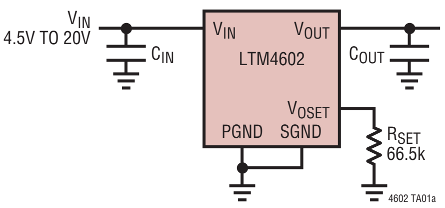
The LTM®4602 is a complete 6A DC/DC step down power supply. Included in the package are the switching controller, power FETs, inductor, and all support components. Operating over an input voltage range of 4.5V to 20V, the LTM4602 supports an output voltage range of 0.6V to 5V, set by a single resistor. This high efficiency design delivers 6A continuous current (8A peak), needing no heat sinks or airflow to meet power specifications. Only bulk input and output capacitors are needed to finish the design.

The low profile package (2.8mm) enables utilization of unused space on the bottom of PC boards for high density point of load regulation. High switching frequency and an adaptive on-time current mode architecture enables a very fast transient response to line and load changes without sacrificing stability. Fault protection features include integrated overvoltage and short circuit protection with a defeatable shutdown timer. A built-in soft-start timer is adjustable with a small capacitor.

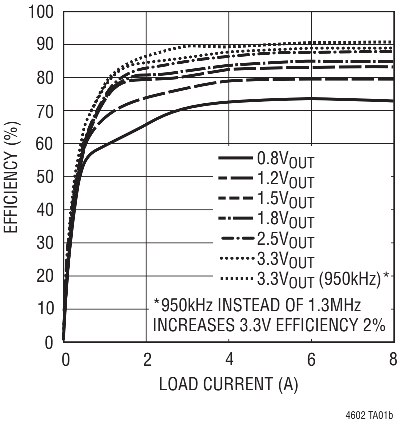
The LTM4602 is packaged in a thermally enhanced, compact (15mm × 15mm) and low profile (2.8mm) over-molded Land Grid Array (LGA) package suitable for automated assembly by standard surface mount equipment. For the 4.5V to 28V input range version, refer to the LTM4602HV.

TYPICAL APPLICATION

6A µModule™ Power Supply with 4.5V to 20V Input



Efficiency vs Load Current with $12V_{IN}$ (FCB = 0)

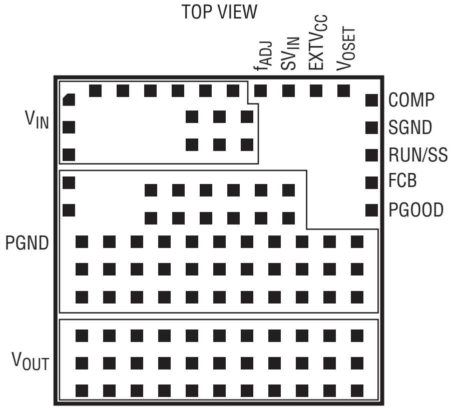


ABSOLUTE MAXIMUM RATINGS

(Note 1)

FCB, $EXTV_{CC}$, PGOOD, RUN/SS, V_{OUT}.......... –0.3V to 6V
V_{IN}, SV_{IN}, f_{ADJ}... –0.3V to 20V
V_{OSET}, COMP.. –0.3V to 2.7V
Operating Temperature Range (Note 2).... –40°C to 85°C
Junction Temperature.. 125°C
Storage Temperature Range................... –55°C to 125°C

PIN CONFIGURATION



LGA PACKAGE
104-LEAD (15mm × 15mm × 2.8mm)
T_{JMAX} = 125°C, θ_{JA} = 15°C/W, θ_{JC} = 6°C/W,
θ_{JA} DERIVED FROM 95mm × 76mm PCB WITH 4 LAYERS
WEIGHT = 1.7g

ORDER INFORMATION

LEAD FREE FINISH	PART MARKING*	PACKAGE DESCRIPTION	TEMPERATURE RANGE
LTM4602EV#PBF	LTM4602V	104-Lead (15mm × 15mm × 2.8mm) LGA	–40°C to 85°C
LTM4602IV#PBF	LTM4602V	104-Lead (15mm × 15mm × 2.8mm) LGA	–40°C to 85°C

Consult LTC Marketing for parts specified with wider operating temperature ranges. *The temperature grade is identified by a label on the shipping container.
Consult LTC Marketing for information on non-standard lead based finish parts.

For more information on lead free part marking, go to: http://www.linear.com/leadfree/
This product is only offered in trays. For more information go to: http://www.linear.com/packaging/

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C to 85°C temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V. External C_{IN} = 120µF, C_{OUT} = 200µF/Ceramic per typical application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$V_{IN(DC)}$	Input DC Voltage		●	4.5		20	V
$V_{OUT(DC)}$	Output Voltage	FCB = 0V V_{IN} = 5V or 12V, V_{OUT} = 1.5V, I_{OUT} = 0A	 ●	 1.478 1.470	 1.50 1.50	 1.522 1.530	 V
Input Specifications							
$V_{IN(UVLO)}$	Under Voltage Lockout Threshold	I_{OUT} = 0A			3.4	4	V
$I_{INRUSH(VIN)}$	Input Inrush Current at Startup	I_{OUT} = 0A. V_{OUT} = 1.5V, FCB = 0 V_{IN} = 5V V_{IN} = 12V			 0.6 0.7		 A A
$I_{Q(VIN)}$	Input Supply Bias Current	I_{OUT} = 0A, $EXTV_{CC}$ Open V_{IN} = 12V, V_{OUT} = 1.5V, FCB = 5V V_{IN} = 12V, V_{OUT} = 1.5V, FCB = 0V V_{IN} = 5V, V_{OUT} = 1.5V, FCB = 5V V_{IN} = 5V, V_{OUT} = 1.5V, FCB = 0V Shutdown, RUN = 0.8V, V_{IN} = 12V			 1.2 42 1.0 52 50	 100	 mA mA mA mA µA

ELECTRICAL CHARACTERISTICS

The ● denotes the specifications which apply over the –40°C to 85°C temperature range, otherwise specifications are at T_A = 25°C, V_{IN} = 12V. Per typical application (front page) configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
$I_{S(VIN)}$	Input Supply Current	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 6A V_{IN} = 12V, V_{OUT} = 3.3V, I_{OUT} = 6A V_{IN} = 5V, V_{OUT} = 1.5V, I_{OUT} = 6 A			0.88 1.80 2.08		A A A
Output Specifications							
I_{OUTDC}	Output Continuous Current Range (See Output Current Derating Curves for Different V_{IN}, V_{OUT} and T_A)	V_{IN} = 12V, V_{OUT} = 1.5V		0		6	A
$\frac{\Delta V_{OUT(LINE)}}{V_{OUT}}$	Line Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A, FCB = 0V, V_{IN} = 4.5V to 20V	●		0.15	0.3	%
$\frac{\Delta V_{OUT(LOAD)}}{V_{OUT}}$	Load Regulation Accuracy	V_{OUT} = 1.5V, I_{OUT} = 0A to 6A, FCB = 0V, V_{IN} = 5V, V_{IN} = 12V (Note 3)	 ●		±0.25 ±0.15	±0.5 ±1.0	% %
$V_{OUT(AC)}$	Output Ripple Voltage	V_{IN} = 12V, V_{OUT} = 1.5V, I_{OUT} = 0A, FCB = 0V			10	15	mV_{P-P}
fs	Output Ripple Voltage Frequency	V_{OUT} = 1.5V, I_{OUT} = 6A, FCB = 0V			850		kHz
t_{START}	Turn-On Time	V_{OUT} = 1.5V, I_{OUT} = 1A V_{IN} = 12V V_{IN} = 5V			 0.5 0.7		 ms ms
ΔV_{OUTLS}	Voltage Drop for Dynamic Load Step	V_{OUT} = 1.5V, Load Step: 0A/µs to 3A/µs C_{OUT} = 22µF 6.3V, 330µF 4V POSCAP, See Table 2			30		mV
t_{SETTLE}	Settling Time for Dynamic Load Step	Load: 10% to 50% to 10% of Full Load			25		µs
I_{OUTPK}	Output Current Limit	Output Voltage in Foldback V_{IN} = 12V, V_{OUT} = 1.5V V_{IN} = 5V, V_{OUT} = 1.5V			 9 9		 A A
Control Stage							
V_{OSET}	Voltage at V_{OSET} Pin	I_{OUT} = 0A, V_{OUT} = 1.5V	●	0.591	0.6	0.609	V
$V_{RUN/SS}$	RUN ON/OFF Threshold			0.8	1.5	2	V
$I_{RUN(C)/SS}$	Soft-Start Charging Current	$V_{RUN/SS}$ = 0V		–0.5	–1.2	–3	µA
$I_{RUN(D)/SS}$	Soft-Start Discharging Current	$V_{RUN/SS}$ = 4V		0.8	1.8	3	µA
$V_{IN} - SV_{IN}$		$EXTV_{CC}$ = 0V, FCB = 0V			100		mV
I_{EXTVCC}	Current into $EXTV_{CC}$ Pin	$EXTV_{CC}$ = 5V, FCB = 0V, V_{OUT} = 1.5V, I_{OUT} = 0A			16		mA
R_{FBHI}	Resistor Between V_{OUT} and V_{OSET} Pins				100		kΩ
V_{FCB}	Forced Continuous Threshold			0.57	0.6	0.63	V
I_{FCB}	Forced Continuous Pin Current	V_{FCB} = 0.6V			–1	–2	µA
PGOOD Output							
ΔV_{OSETH}	PGOOD Upper Threshold	V_{OSET} Rising		7.5	10	12.5	%
ΔV_{OSETL}	PGOOD Lower Threshold	V_{OSET} Falling		–7.5	–10	–12.5	%
$\Delta V_{OSET(HYS)}$	PGOOD Hysteresis	V_{OSET} Returning			2		%
V_{PGL}	PGOOD Low Voltage	I_{PGOOD} = 5mA			0.15	0.4	V

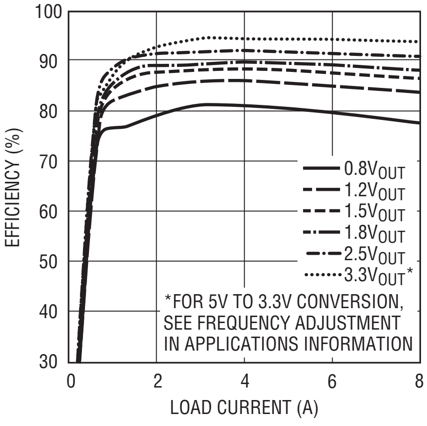
Note 1: Stresses beyond those listed under Absolute Maximum Ratings may cause permanent damage to the device. Exposure to any Absolute Maximum Rating condition for extended periods may affect device reliability and lifetime.

Note 2: The LTM4602E is guaranteed to meet performance specifications from 0°C to 85°C. Specifications over the –40°C to 85°C operating temperature range are assured by design, characterization and correlation with statistical process controls. The LTM4602I is guaranteed over the –40°C to 85°C temperature range.

Note 3: Test assumes current derating versus temperature.

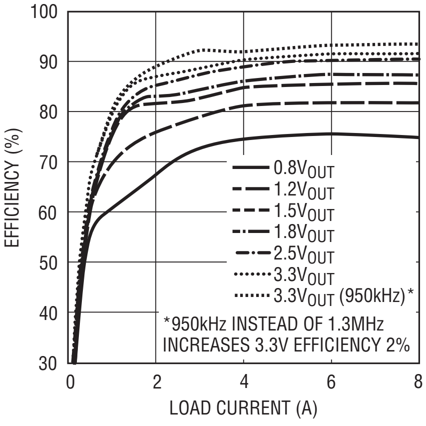
TYPICAL PERFORMANCE CHARACTERISTICS (See Figure 21 for all curves)

Efficiency vs Load Current with 5V_{IN} (FCB = 0)



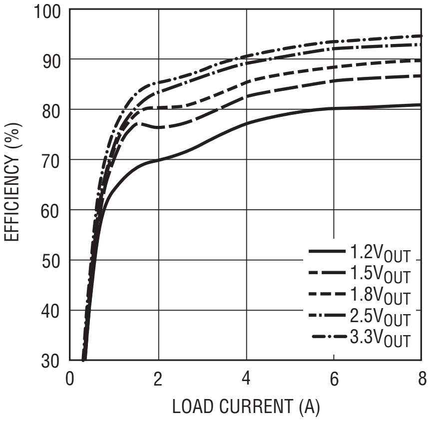
4602 G01

Efficiency vs Load Current with 12V_{IN} (FCB = 0)



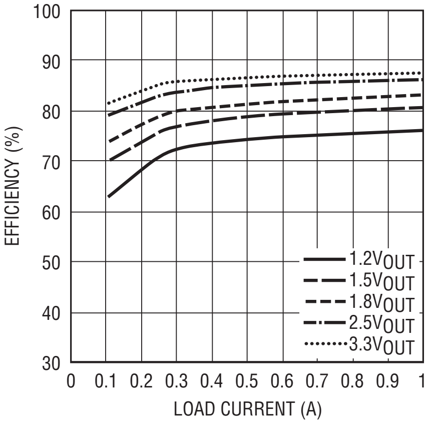
4602 G02

Efficiency vs Load Current with 20V_{IN} (FCB = 0)



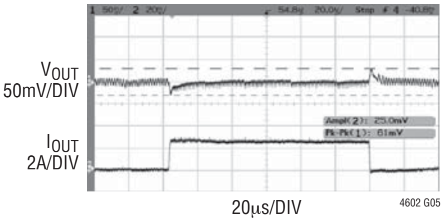
4602 G03

Light Load Efficiency vs Load Current with 12V_{IN} (FCB > 0.7V, <5V)



4602 G04

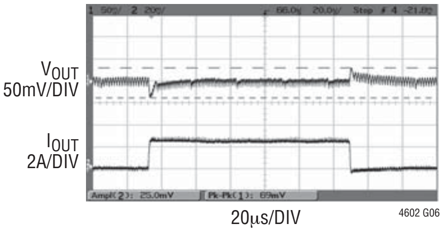
1.2V Transient Response



4602 G05

1.2V AT 3A/µs LOAD STEP
C_{OUT} = 1 × 22µF, 6.3V CERAMICS
330µF, 4V SANYO POSCAP

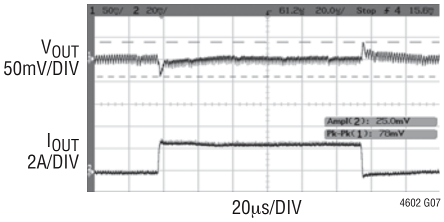
1.5V Transient Response



4602 G06

1.5V AT 3A/µs LOAD STEP
C_{OUT} = 1 × 22µF, 6.3V CERAMICS
330µF, 4V SANYO POSCAP

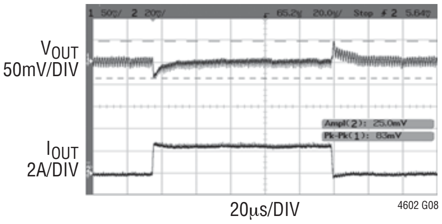
1.8V Transient Response



4602 G07

1.8V AT 3A/µs LOAD STEP
C_{OUT} = 1 × 22µF, 6.3V CERAMICS
330µF, 4V SANYO POSCAP

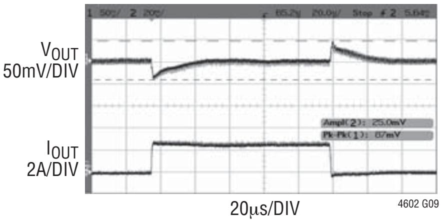
2.5V Transient Response



4602 G08

2.5V AT 3A/µs LOAD STEP
C_{OUT} = 1 × 22µF, 6.3V CERAMICS
330µF, 4V SANYO POSCAP

3.3V Transient Response

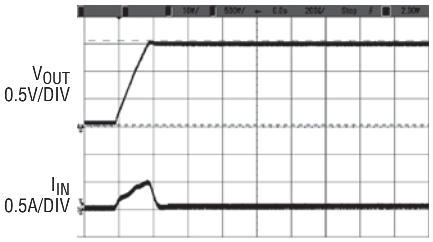


4602 G09

3.3V AT 3A/µs LOAD STEP
C_{OUT} = 1 × 22µF, 6.3V CERAMICS
330µF, 4V SANYO POSCAP

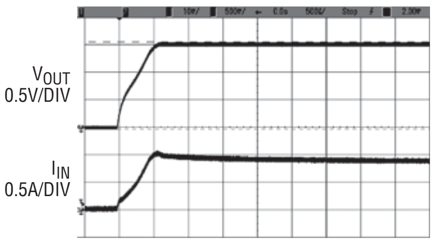
TYPICAL PERFORMANCE CHARACTERISTICS (See Figure 21 for all curves)

Start-Up, No Load, I_{OUT} = 0A



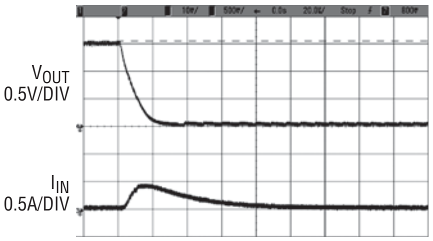
V_{IN} = 12V 200µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 1 × 22µF, 6.3V X5R
330µF, 4V SANYO POSCAP
NO EXTERNAL SOFT-START CAPACITOR

Start-Up, I_{OUT} = 6A (Resistive Load)



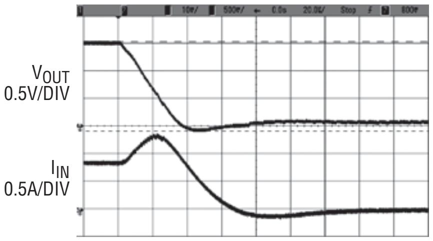
V_{IN} = 12V 500µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 1 × 22µF, 6.3V X5R
330µF, 4V SANYO POSCAP
NO EXTERNAL SOFT-START CAPACITOR

Short-Circuit Protection, I_{OUT} = 0A



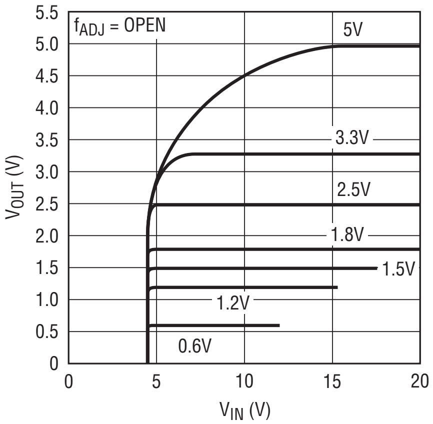
V_{IN} = 12V 20µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 1 × 22µF, 6.3V X5R
330µF, 4V SANYO POSCAP
NO EXTERNAL SOFT-START CAPACITOR

Short-Circuit Protection, I_{OUT} = 6A



V_{IN} = 12V 20µs/DIV
V_{OUT} = 1.5V
C_{OUT} = 1 × 22µF, 6.3V X5R
330µF, 4V SANYO POSCAP
NO EXTERNAL SOFT-START CAPACITOR

V_{IN} to V_{OUT} Step-Down Ratio



SEE FREQUENCY ADJUSTMENT DISCUSSION
FOR $12V_{IN}$ TO $5V_{OUT}$ AND $5V_{IN}$ TO $3.3V_{OUT}$
CONVERSION

4602 G14

PIN FUNCTIONS (See Package Description for Pin Assignment)

V_{IN} (Bank 1): Power Input Pins. Apply input voltage between these pins and PGND pins. Recommend placing input decoupling capacitance directly between V_{IN} pins and PGND pins.

f_{ADJ} (Pin A15): A 110k resistor from V_{IN} to this pin sets the one-shot timer current, thereby setting the switching frequency. The LTM4602 switching frequency is typically 850kHz. An external resistor to ground can be selected to reduce the one-shot timer current, thus lower the switching frequency to accommodate a higher duty cycle step down requirement. See the applications section.

SV_{IN} (Pin A17): Supply Pin for Internal PWM Controller. Leave this pin open or add additional decoupling capacitance.

$EXTV_{CC}$ (Pin A19): External 5V supply pin for controller. If left open or grounded, the internal 5V linear regulator will power the controller and MOSFET drivers. For high input voltage applications, connecting this pin to an external 5V will reduce the power loss in the power module. The $EXTV_{CC}$ voltage should never be higher than V_{IN}.

V_{OSET} (Pin A21): The Negative Input of The Error Amplifier. Internally, this pin is connected to V_{OUT} with a 100k precision resistor. Different output voltages can be programmed with additional resistors between the V_{OSET} and SGND pins.

COMP (Pin B23): Current Control Threshold and Error Amplifier Compensation Point. The current comparator threshold increases with this control voltage. The voltage ranges from 0V to 2.4V with 0.8V corresponding to zero sense voltage (zero current).

SGND (Pin D23): Signal Ground Pin. All small-signal components should connect to this ground, which in turn connects to PGND at one point.

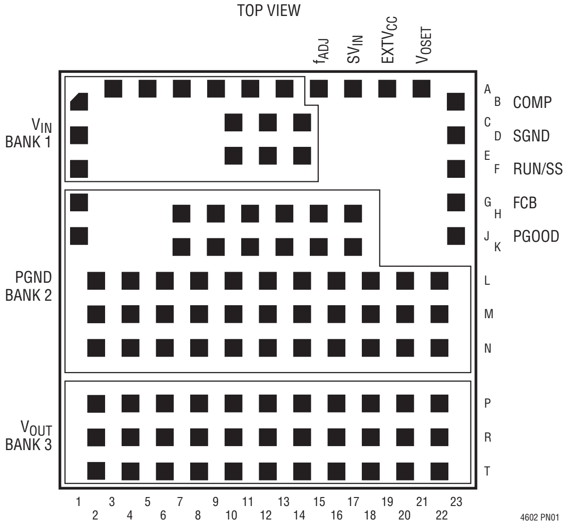
RUN/SS (Pin F23): Run and Soft-Start Control. Forcing this pin below 0.8V will shut down the power supply. Inside the power module, there is a 1000pF capacitor which provides approximately 0.7ms soft-start time with 200µF output capacitance. Additional soft-start time can be achieved by adding additional capacitance between the RUN/SS and SGND pins. The internal short-circuit latchoff can be disabled by adding a resistor between this pin and the V_{IN} pin. This pullup resistor must supply a minimum 5µA pull up current.

FCB (Pin G23): Forced Continuous Input. Grounding this pin enables forced continuous mode operation regardless of load conditions. Tying this pin above 0.63V enables discontinuous conduction mode to achieve high efficiency operation at light loads. There is an internal 4.75k resistor between the FCB and SGND pins.

PGOOD (Pin J23): Output Voltage Power Good Indicator. When the output voltage is within 10% of the nominal voltage, the PGOOD is open drain output. Otherwise, this pin is pulled to ground.

PGND (Bank 2): Power ground pins for both input and output returns.

V_{OUT} (Bank 3): Power Output Pins. Apply output load between these pins and PGND pins. Recommend placing High Frequency output decoupling capacitance directly between these pins and PGND pins.



SIMPLIFIED BLOCK DIAGRAM

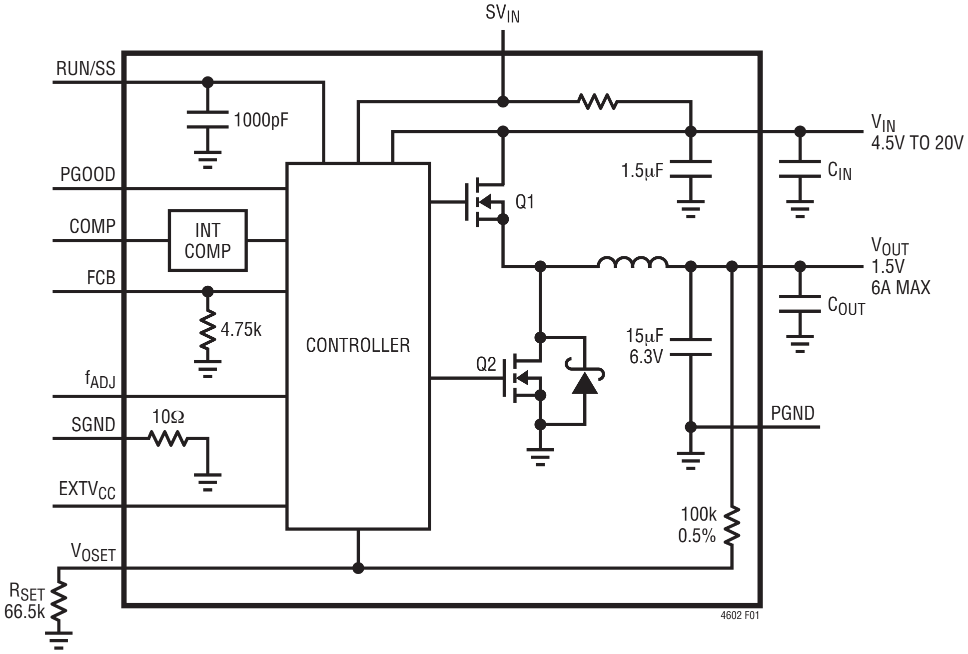


Figure 1. Simplified LTM4602 Block Diagram

DECOUPLING REQUIREMENTS T_A = 25°C, V_{IN} = 12V. Use Figure 1 configuration.

SYMBOL	PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
C_{IN}	External Input Capacitor Requirement (V_{IN} = 4.5V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 6A		20			μF
C_{OUT}	External Output Capacitor Requirement (V_{IN} = 4.5V to 20V, V_{OUT} = 1.5V)	I_{OUT} = 6A, Refer to Table 2 in the Applications Information Section		100	200		μF

OPERATION

μModule Description

The LTM4602 is a standalone nonisolated synchronous switching DC/DC power supply. It can deliver up to 6A of DC output current with only bulk external input and output capacitors. This module provides a precisely regulated output voltage programmable via one external resistor from $0.6V_{DC}$ to $5.0V_{DC}$, not to exceed 80% of the input voltage. The input voltage range is 4.5V to 20V. A simplified block diagram is shown in Figure 1 and the typical application schematic is shown in Figure 21.

The LTM4602 contains an integrated LTC constant on-time current-mode regulator, ultralow $R_{DS(ON)}$ FETs with fast switching speed and integrated Schottky diode. The typical switching frequency is 850kHz at full load. With current mode control and internal feedback loop compensation, the LTM4602 module has sufficient stability margins and good transient performance under a wide range of operating conditions and with a wide range of output capacitors, even all ceramic output capacitors (X5R or X7R).

Current mode control provides cycle-by-cycle fast current limit. In addition, foldback current limiting is provided in an overcurrent condition while V_{OSET} drops. Also, the LTM4602 has defeatable short-circuit latch off. Internal overvoltage and undervoltage comparators pull the open-drain PGOOD output low if the output feedback voltage exits a ±10% window around the regulation point. Furthermore, in an overvoltage condition, internal top FET Q1 is turned off and bottom FET Q2 is turned on and held on until the overvoltage condition clears.

Pulling the RUN/SS pin low forces the controller into its shutdown state, turning off both Q1 and Q2. Releasing the pin allows an internal 1.2μA current source to charge up the soft-start capacitor. When this voltage reaches 1.5V, the controller turns on and begins switching.

At low load current the module works in continuous current mode by default to achieve minimum output voltage ripple. It can be programmed to operate in discontinuous current mode for improved light load efficiency when the FCB pin is pulled up above 0.8V and no higher than 6V. The FCB pin has a 4.75k resistor to ground, so a resistor to V_{IN} can set the voltage on the FCB pin.

When $EXTV_{CC}$ pin is grounded or open, an integrated 5V linear regulator powers the controller and MOSFET gate drivers. If a minimum 4.7V external bias supply is applied on the $EXTV_{CC}$ pin, the internal regulator is turned off, and an internal switch connects $EXTV_{CC}$ to the gate driver voltage. This eliminates the linear regulator power loss with high input voltage, reducing the thermal stress on the controller. The maximum voltage on $EXTV_{CC}$ pin is 6V. The $EXTV_{CC}$ voltage should never be higher than the V_{IN} voltage. Also $EXTV_{CC}$ must be sequenced after V_{IN}.

APPLICATIONS INFORMATION

The typical LTM4602 application circuit is shown in Figure 21. External component selection is primarily determined by the maximum load current and output voltage.

Output Voltage Programming and Margining

The PWM controller of the LTM4602 has an internal 0.6V reference voltage. As shown in the block diagram, a 100k/0.5% internal feedback resistor connects V_{OUT} and V_{OSET} pins. Adding a resistor R_{SET} from V_{OSET} pin to SGND pin programs the output voltage:

$$V_{OUT} = 0.6V \bullet \frac{100k + R_{SET}}{R_{SET}}$$

Table 1 shows the standard values of 1% R_{SET} resistor for typical output voltages:

Table 1

R_{SET} (kΩ)	Open	100	66.5	49.9	43.2	31.6	22.1	13.7
V_{OUT} (V)	0.6	1.2	1.5	1.8	2	2.5	3.3	5

Voltage margining is the dynamic adjustment of the output voltage to its worst case operating range in production testing to stress the load circuitry, verify control/protection functionality of the board and improve the system reliability. Figure 2 shows how to implement margining function with the LTM4602. In addition to the feedback resistor R_{SET}, several external components are added. Turn off both transistor Q_{UP} and Q_{DOWN} to disable the margining. When Q_{UP} is on and Q_{DOWN} is off, the output voltage is margined up. The output voltage is margined down when Q_{DOWN} is on and Q_{UP} is off. If the output voltage V_{OUT} needs to be margined up/down by ±M%, the resistor values of R_{UP} and R_{DOWN} can be calculated from the following equations:

$$\frac{(R_{SET} \| R_{UP}) \bullet V_{OUT} \bullet (1 + M\%)}{(R_{SET} \| R_{UP}) + 100k\Omega} = 0.6V$$

$$\frac{R_{SET} \bullet V_{OUT} \bullet (1 - M\%)}{R_{SET} + (100k\Omega \| R_{DOWN})} = 0.6V$$

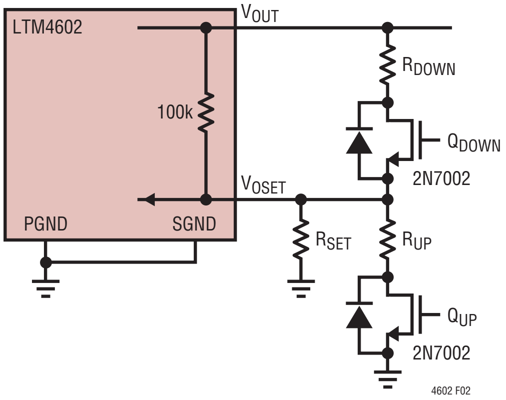


Figure 2. LTM4602 Margining Implementation

Input Capacitors

The LTM4602 µModule should be connected to a low AC-impedance DC source. High frequency, low ESR input capacitors are required to be placed adjacent to the module. In Figure 21, the bulk input capacitor C_{IN} is selected for its ability to handle the large RMS current into the converter. For a buck converter, the switching duty cycle can be estimated as:

$$D = \frac{V_{OUT}}{V_{IN}}$$

Without considering the inductor current ripple, the RMS current of the input capacitor can be estimated as:

$$I_{CIN(RMS)} = \frac{I_{OUT(MAX)}}{\eta\%} \bullet \sqrt{D \bullet (1 - D)}$$

In the above equation, η% is the estimated efficiency of the power module. C1 can be a switcher-rated electrolytic aluminum capacitor, OS-CON capacitor or high volume ceramic capacitors. Note the capacitor ripple current ratings are often based on only 2000 hours of life. This makes it advisable to properly derate the input capacitor, or choose a capacitor rated at a higher temperature than required. Always contact the capacitor manufacturer for derating requirements.

In Figure 21, the input capacitors are used as high frequency input decoupling capacitors. In a typical 6A output application, 1-2 pieces of very low ESR X5R or X7R, 10µF ceramic capacitors are recommended. This decoupling capacitor should be placed directly adjacent the module input pins in the PCB layout to minimize the trace inductance and high frequency AC noise.

APPLICATIONS INFORMATION

Output Capacitors

The LTM4602 is designed for low output voltage ripple. The bulk output capacitors C_{OUT} is chosen with low enough effective series resistance (ESR) to meet the output voltage ripple and transient requirements. C_{OUT} can be low ESR tantalum capacitor, low ESR polymer capacitor or ceramic capacitor (X5R or X7R). The typical capacitance is 200µF if all ceramic output capacitors are used. The internally optimized loop compensation provides sufficient stability margin for all ceramic capacitors applications. Additional output filtering may be required by the system designer, if further reduction of output ripple or dynamic transient spike is required. Refer to Table 2 for an output capacitance matrix for each output voltage droop, peak to peak deviation and recovery time during a 3A/µs transient with a specific output capacitance.

Fault Conditions: Current Limit and Overcurrent Foldback

The LTM4602 has a current mode controller, which inherently limits the cycle-by-cycle inductor current not only in steady-state operation, but also in transient.

To further limit current in the event of an over load condition, the LTM4602 provides foldback current limiting. If the output voltage falls by more than 50%, then the maximum output current is progressively lowered to about one sixth of its full current limit value.

Soft-Start and Latchoff with the RUN/SS pin

The RUN/SS pin provides a means to shut down the LTM4602 as well as a timer for soft-start and overcurrent latchoff. Pulling the RUN/SS pin below 0.8V puts the LTM4602 into a low quiescent current shutdown ($I_Q \leq$ 100µA). Releasing the pin allows an internal 1.2µA current source to charge up the timing capacitor C_{SS}. Inside LTM4602, there is an internal 1000pF capacitor from RUN/SS pin to ground. If RUN/SS pin has an external capacitor C_{SS_EXT} to ground, the delay before starting is about:

$$t_{DELAY} = \frac{1.5V}{1.2\mu A} \bullet (C_{SS\_EXT} + 1000pF)$$

When the voltage on RUN/SS pin reaches 1.5V, the LTM4602 internal switches are operating with a clamping of the maximum output inductor current limited by the RUN/SS pin total soft-start capacitance. As the RUN/SS pin voltage rises to 3V, the soft-start clamping of the inductor current is released.

V_{IN} to V_{OUT} Step-Down Ratios

There are restrictions in the maximum V_{IN} to V_{OUT} step down ratio that can be achieved for a given input voltage. These constraints are shown in the Typical Performance Characteristics curves labeled "V_{IN} to V_{OUT} Step-Down Ratio". Note that additional thermal derating may apply. See the Thermal Considerations and Output Current Derating sections of this data sheet.

APPLICATIONS INFORMATION

Table 2. Output Voltage Response Versus Component Matrix (Refer to Figure 21), 0A to 3A Step (Typical Values)

TYPICAL MEASURED VALUES

C_{OUT1} VENDORS	PART NUMBER	C_{OUT2} VENDORS	PART NUMBER
TDK	C4532X5R0J107MZ (100µF,6.3V)	SANYO POSCAP	6TPE330MIL (330µF, 6.3V)
TAIYO YUDEN	JMK432BJ107MU-T (100µF, 6.3V)	SANYO POSCAP	2R5TPE470M9 (470µF, 2.5V)
TAIYO YUDEN	JMK316BJ226ML-T501 (22µF, 6.3V)	SANYO POSCAP	4TPE470MCL (470µF, 4V)

V_{OUT} (V)	C_{IN} (CERAMIC)	C_{IN} (BULK)	C_{OUT1} (CERAMIC)	C_{OUT2} (BULK)	C_{COMP}	C3	V_{IN} (V)	DROOP (mV)	PEAK TO PEAK (mV)	RECOVERY TIME (µs)	LOAD STEP (A/µs)
1.2	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	5	50	60	25	3
1.2	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	100pF	5	30	60	20	3
1.2	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	5	25	54	20	3
1.2	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	5	25	55	20	3
1.2	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	12	30	60	25	3
1.2	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	100pF	12	25	54	20	3
1.2	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	12	25	50	20	3
1.2	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	12	25	55	20	3
1.5	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	5	25	50	25	3
1.5	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	100pF	5	25	54	20	3
1.5	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	5	28	59	20	3
1.5	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	5	26	59	20	3
1.5	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	12	25	55	25	3
1.5	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	100pF	12	25	54	20	3
1.5	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	12	28	59	20	3
1.5	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	12	26	59	20	3
1.8	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	5	25	54	30	3
1.8	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	100pF	5	25	50	20	3
1.8	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	5	25	50	20	3
1.8	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	5	29	60	20	3
1.8	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	100pF	12	25	50	30	3
1.8	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 2.5V	NONE	100pF	12	25	50	20	3
1.8	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	100pF	12	25	50	20	3
1.8	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	100pF	12	29	60	20	3
2.5	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 4V	NONE	220pF	5	25	50	30	3
2.5	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	220pF	5	25	50	30	3
2.5	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	220pF	5	25	50	30	3
2.5	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	220pF	5	25	50	25	3
2.5	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 4V	NONE	220pF	12	25	50	30	3
2.5	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	220pF	12	25	50	30	3
2.5	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	220pF	12	25	50	30	3
2.5	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	220pF	12	27	54	25	3
3.3	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	220pF	7	32	64	30	3
3.3	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 4V	NONE	220pF	7	30	60	30	3
3.3	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	220pF	7	30	60	35	3
3.3	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	220pF	7	32	64	25	3
3.3	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	470µF 4V	NONE	220pF	12	38	58	30	3
3.3	2 × 10µF 25V	150µF 35V	3 × 22µF 6.3V	470µF 4V	NONE	220pF	12	30	60	35	3
3.3	2 × 10µF 25V	150µF 35V	2 × 100µF 6.3V	330µF 6.3V	NONE	220pF	12	30	60	30	3
3.3	2 × 10µF 25V	150µF 35V	4 × 100µF 6.3V	NONE	NONE	220pF	12	32	64	25	3
5	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	NONE	NONE	100pF	15	80	160	25	3
5	2 × 10µF 25V	150µF 35V	1 × 100µF 6.3V	NONE	NONE	100pF	20	80	160	25	3

APPLICATIONS INFORMATION

After the controller has been started and given adequate time to charge up the output capacitor, C_{SS} is used as a short-circuit timer. After the RUN/SS pin charges above 4V, if the output voltage falls below 75% of its regulated value, then a short-circuit fault is assumed. A 1.8μA current then begins discharging C_{SS}. If the fault condition persists until the RUN/SS pin drops to 3.5V, then the controller turns off both power MOSFETs, shutting down the converter permanently. The RUN/SS pin must be actively pulled down to ground in order to restart operation.

The overcurrent protection timer requires the soft-start timing capacitor C_{SS} be made large enough to guarantee that the output regulation by the time C_{SS} has reached the 4V threshold. In general, this will depend upon the size of the output capacitance, output voltage and load current characteristic. A minimum external soft-start capacitor can be estimated from:

$$C_{SS\_EXT} + 1000pF > C_{OUT} \bullet V_{OUT}(10^{-3}[F/V_S])$$

Generally 0.1μF is more than sufficient.

Since the load current is already limited by the current mode control and current foldback circuitry during a short circuit, overcurrent latchoff operation is NOT always needed or desired, especially if the output has large capacitance or the load draws high current during start up. The latchoff feature can be overridden by a pull-up current greater than 5μA but less than 80μA to the RUN/SS pin. The additional current prevents the discharge of C_{SS} during a fault and also shortens the soft-start period. Using a resistor from RUN/SS pin to V_{IN} is a simple solution to defeat latchoff. Any pull-up network must be able to maintain RUN/SS above 4V maximum latchoff threshold and overcome the 4μA maximum discharge current. Figure 3 shows a conceptual drawing of V_{RUN} during start-up and short circuit.

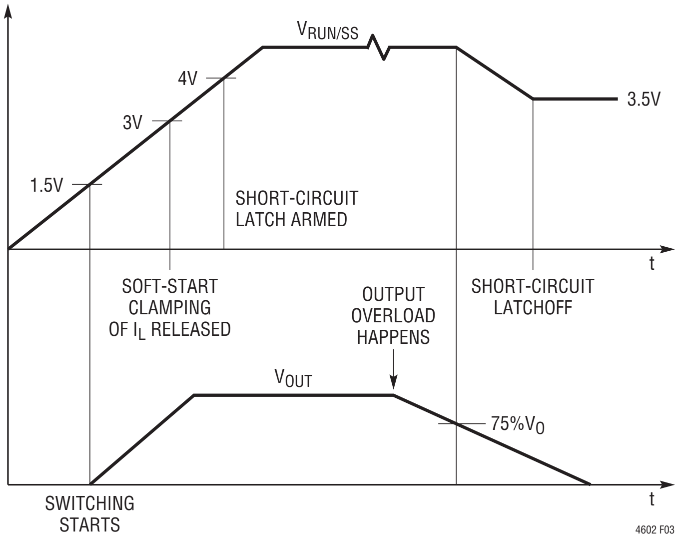
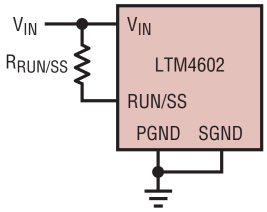


Figure 3. RUN/SS Pin Voltage During Startup and Short-Circuit Protection



RECOMMENDED VALUES FOR $R_{RUN/SS}$

V_{IN}	$R_{RUN/SS}$
4.5V TO 5.5V	50k
10.8V TO 13.8V	150k
16V TO 20V	330k

4602 F04

Figure 4. Defeat Short-Circuit Latchoff with a Pull-Up Resistor to V_{IN}

APPLICATIONS INFORMATION

Enable

The RUN/SS pin can be driven from logic as shown in Figure 5. This function allows the LTM4602 to be turned on or off remotely. The $\overline{\text{ON}}$ signal can also control the sequence of the output voltage.

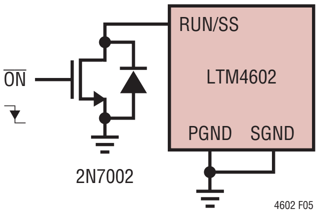


Figure 5. Enable Circuit with External Logic

Output Voltage Tracking

For the applications that require output voltage tracking, several LTM4602 modules can be programmed by the power supply tracking controller such as the LTC2923. Figure 6 shows a typical schematic with LTC2923. Coincident, ratiometric and offset tracking for V_{OUT} rising and falling can be implemented with different sets of resistor values. See the LTC2923 data sheet for more details.

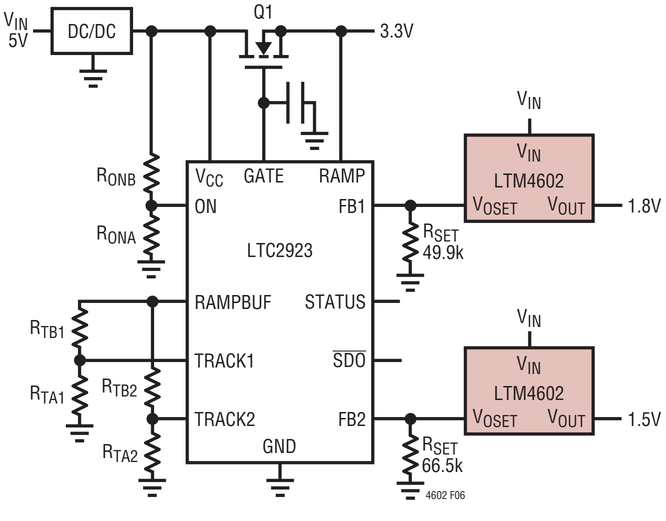


Figure 6. Output Voltage Tracking with the LTC2923 Controller

$EXTV_{CC}$ Connection

An internal low dropout regulator produces an internal 5V supply that powers the control circuitry and FET drivers. Therefore, if the system does not have a 5V power rail, the LTM4602 can be directly powered by V_{IN}. The gate driver current through LDO is about 18mA. The internal LDO power dissipation can be calculated as:

$$P_{LDO\_LOSS} = 18mA \bullet (V_{IN} - 5V)$$

The LTM4602 also provides an external gate driver voltage pin $EXTV_{CC}$. If there is a 5V rail in the system, it is recommended to connect $EXTV_{CC}$ pin to the external 5V rail. Whenever the $EXTV_{CC}$ pin is above 4.7V, the internal 5V LDO is shut off and an internal 50mA P-channel switch connects the $EXTV_{CC}$ to internal 5V. Internal 5V is supplied from $EXTV_{CC}$ until this pin drops below 4.5V. Do not apply more than 6V to the $EXTV_{CC}$ pin and ensure that $EXTV_{CC} < V_{IN}$. The following list summaries the possible connections for $EXTV_{CC}$:

1. $EXTV_{CC}$ grounded. Internal 5V LDO is always powered from the internal 5V regulator.

2. $EXTV_{CC}$ connected to an external supply. Internal LDO is shut off. A high efficiency supply compatible with the MOSFET gate drive requirements (typically 5V) can improve overall efficiency. With this connection, it is always required that the $EXTV_{CC}$ voltage can not be higher than V_{IN} pin voltage.

Discontinuous Operation and FCB Pin

The FCB pin determines whether the internal bottom MOSFET remains on when the inductor current reverses. There is an internal 4.75k pull-down resistor connecting this pin to ground. The default light load operation mode is forced continuous (PWM) current mode. This mode provides minimum output voltage ripple.

In the application where the light load efficiency is important, tying the FCB pin above 0.6V threshold enables discontinuous operation where the bottom MOSFET turns off when inductor current reverses. Therefore, the conduc-

APPLICATIONS INFORMATION

tion loss is minimized and light load efficiency is improved. The penalty is that the controller may skip cycle and the output voltage ripple increases at light load.

Paralleling Operation with Load Sharing

Two or more LTM4602 modules can be paralleled to provide higher than 6A output current. Figure 7 shows the necessary interconnection between two paralleled modules. The OPTI-LOOP® current mode control ensures good current sharing among modules to balance the thermal stress. The new feedback equation for two or more LTM4602s in parallel is:

$$V_{OUT} = 0.6V \bullet \frac{\frac{100k}{N} + R_{SET}}{R_{SET}}$$

where N is the number of LTM4602s in parallel.

Thermal Considerations and Output Current Derating

The power loss curves in Figures 8 and 13 can be used in coordination with the load current derating curves in Figures 9 to 12, and Figures 14 to 15 for calculating an approximate θ_{JA} for the module with various heat sinking methods. Thermal models are derived from several temperature measurements at the bench, and thermal modeling analysis. Application Note 103 provides a detailed explanation of the analysis for the thermal models, and the derating curves. Tables 3 and 4 provide a summary of the equivalent θ_{JA} for the noted conditions. These equivalent θ_{JA} parameters are correlated to the measured values, and improve with air-flow. The case temperature is maintained at 100°C or below for the derating curves. This allows for 4W maximum power dissipation in the total module with top and bottom heat sinking, and 2W power dissipation through the top of the module with an approximate θ_{JC} between 6°C/W to 9°C/W. This equates to a total of 124°C at the junction of the device. The θ_{JA} values in Tables 3 and 4 can be used to derive the derating curves for other output voltages.

Safety Considerations

The LTM4602 modules do not provide isolation from V_{IN} to V_{OUT}. There is no internal fuse. If required, a slow blow fuse with a rating twice the maximum input current should be provided to protect each unit from catastrophic failure.

OPTI-LOOP is a registered trademark of Linear Technology Corporation.

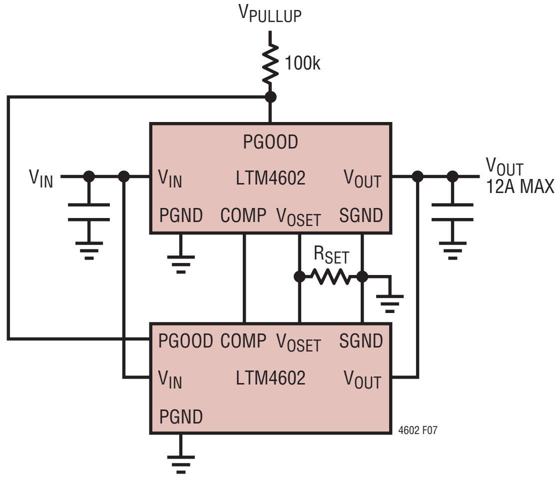


Figure 7. Parallel Two µModules with Load Sharing

APPLICATIONS INFORMATION

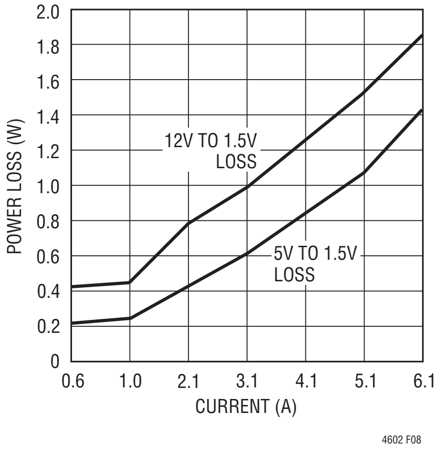


Figure 8. 1.5V Power Loss vs Load Current

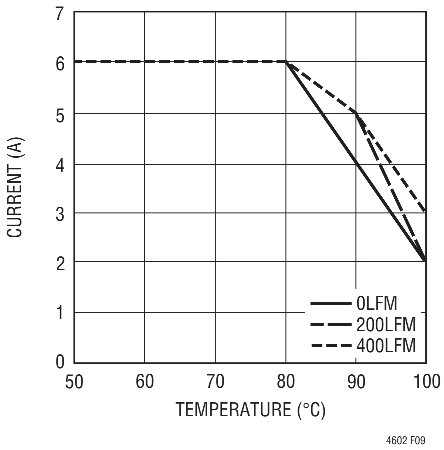


Figure 9. 5V to 1.5V, No Heat Sink

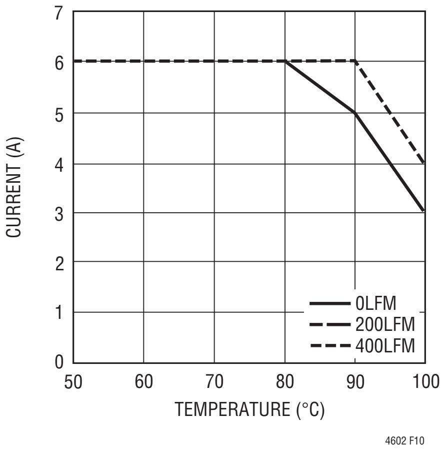


Figure 10. 5V to 1.5V, BGA Heat Sink

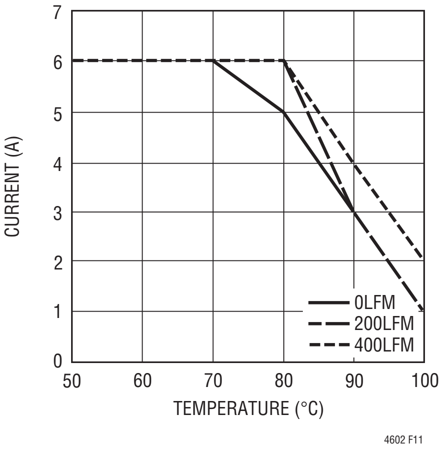


Figure 11. 12V to 1.5V, No Heat Sink

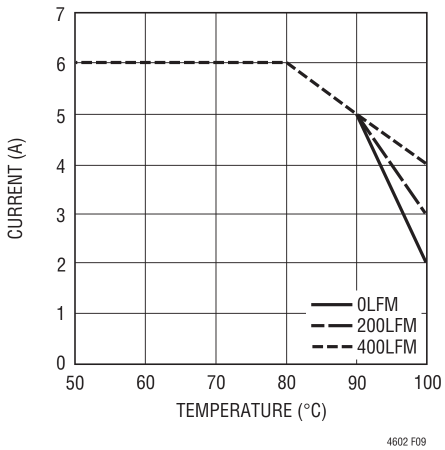


Figure 12. 12v to 1.5V, BGA Heat Sink

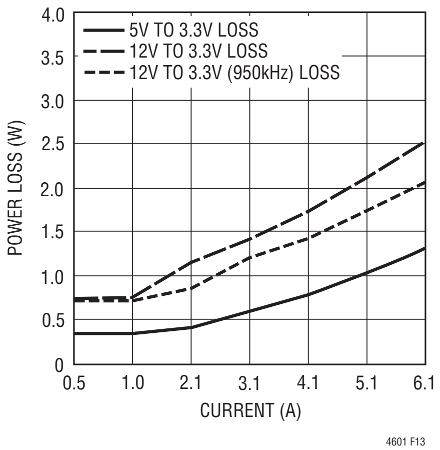


Figure 13. 3.3V Power Loss vs Load Current

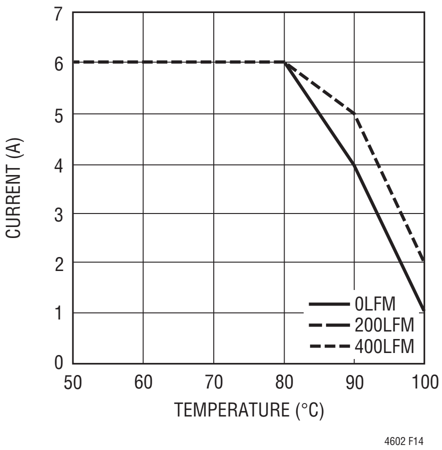


Figure 14. 5V to 3.3V, No Heat Sink

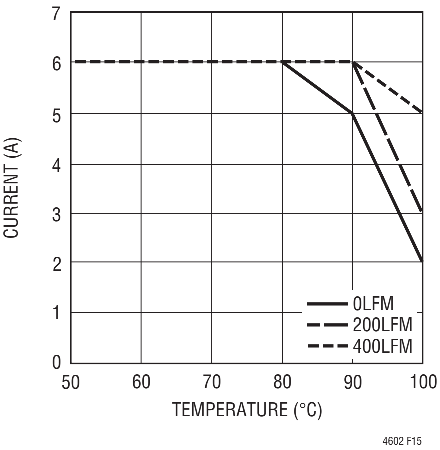


Figure 15. 5V to 3.3V, BGA Heat Sink

APPLICATIONS INFORMATION

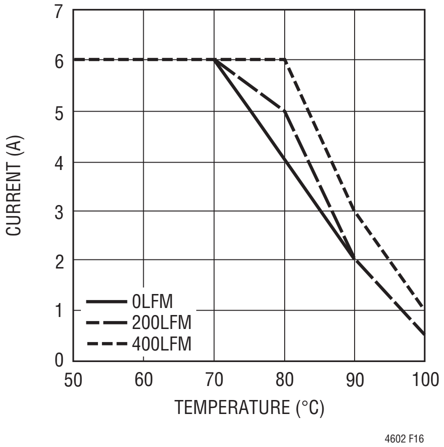


Figure 16. 12V to 3.3V, No Heat Sink

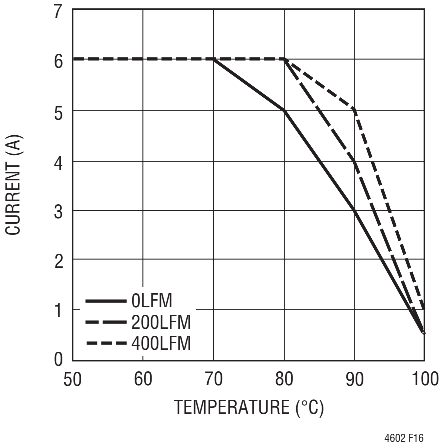


Figure 17. 12V to 3.3V, BGA Heat Sink

Table 3. 1.5V Output

AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
0	None	15.2
200	None	14
400	None	12
0	BGA Heat Sink	13.9
200	BGA Heat Sink	11.3
400	BGA Heat Sink	10.25

Table 4. 3.3V Output

AIR FLOW (LFM)	HEAT SINK	θ_{JA} (°C/W)
0	None	15.2
200	None	14.6
400	None	13.4
0	BGA Heat Sink	13.9
200	BGA Heat Sink	11.1
400	BGA Heat Sink	10.5

Layout Checklist/Example

The high integration of the LTM4602 makes the PCB board layout very simple and easy. However, to optimize its electrical and thermal performance, some layout considerations are still necessary.

- Use large PCB copper areas for high current path, including V_{IN}, PGND and V_{OUT}. It helps to minimize the PCB conduction loss and thermal stress.
- Place high frequency ceramic input and output capacitors next to the V_{IN}, PGND and V_{OUT} pins to minimize high frequency noise.
- Place a dedicated power ground layer underneath the unit.
- To minimize the via conduction loss and reduce module thermal stress, use multiple vias for interconnection between top layer and other power layers.
- Do not put vias directly on pads unless they are capped.
- Use a separated SGND ground copper area for components connected to signal pins. Connect the SGND to PGND underneath the unit.

Figure 18 gives a good example of the recommended layout.

LTM4602 Frequency Adjustment

The LTM4602 is designed to typically operate at 850kHz across most input and output conditions. The control architecture is constant on time valley mode current control. The f_{ADJ} pin is typically left open or decoupled with an optional 1000pF capacitor. The switching frequency has been optimized to maintain constant output ripple over the operating conditions. The equations for setting the operating frequency are set around a programmable constant on time. This on time is developed by a programmable current into an on board 10pF capacitor that establishes a ramp that is compared to a voltage threshold equal to the output voltage up to a 2.4V clamp. This I_{ON} current is equal to: $I_{ON} = (V_{IN} – 0.7V)/110k$, with the 110k onboard resistor

APPLICATIONS INFORMATION

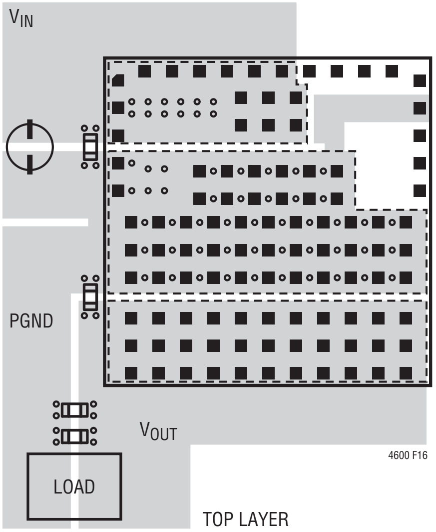


Figure 18. Recommended PCB Layout

from V_{IN} to f_{ADJ}. The on time is equal to $t_{ON} = (V_{OUT}/I_{ON}) \bullet 10pF$ and $t_{OFF} = t_s - t_{ON}$. The frequency is equal to: Freq. = DC/t_{ON}. The I_{ON} current is proportional to V_{IN}, and the regulator duty cycle is inversely proportional to V_{IN}, therefore the step-down regulator will remain relatively constant frequency as the duty cycle adjustment takes place with lowering V_{IN}. The on time is proportional to V_{OUT} up to a 2.4V clamp. This will hold frequency relatively constant with different output voltages up to 2.4V. The regulator switching period is comprised of the on time and off time as depicted in Figure 19.

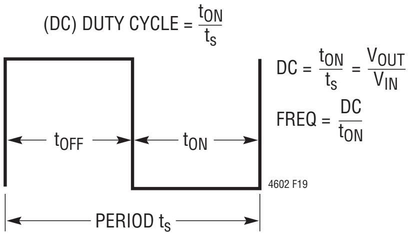


Figure 19. LTM4602 Switching Period

The LTM4602 has a minimum (t_{ON}) on time of 100 nanoseconds and a minimum (t_{OFF}) off time of 400 nanoseconds. The 2.4V clamp on the ramp threshold as a function of V_{OUT} will cause the switching frequency to increase by the ratio of V_{OUT}/2.4V for 3.3V and 5V outputs. This is due to the fact the on time will not increase as V_{OUT} increases past 2.4V. Therefore, if the nominal switching frequency is 850kHz, then the switching frequency will increase to ~1.2MHz for 3.3V, and ~1.7MHz for 5V outputs due to Frequency = (DC/t_{ON}) When the switching frequency increases to 1.2MHz, then the time period t_S is reduced to ~833 nanoseconds and at 1.7MHz the switching period reduces to ~588 nanoseconds. When higher duty cycle conversions like 5V to 3.3V and 12V to 5V need to be accommodated, then the switching frequency can be lowered to alleviate the violation of the 400ns minimum off time. Since the total switching period is $t_S = t_{ON} + t_{OFF}$, t_{OFF} will be below the 400ns minimum off time. A resistor from the f_{ADJ} pin to ground can shunt current away from the on time generator, thus allowing for a longer on time and a lower switching frequency. 12V to 5V and 5V to 3.3V derivations are explained in the data sheet to lower switching frequency and accommodate these step-down conversions.

Equations for setting frequency for 12V to 5V:

$I_{ON} = (V_{IN} - 0.7V)/110k$; $I_{ON} = 103\mu A$

frequency = $(I_{ON}/[2.4V \bullet 10pF]) \bullet DC = 1.79MHz$; DC = duty cycle, duty cycle is (V_{OUT}/V_{IN})

$t_S = t_{ON} + t_{OFF}$, t_{ON} = on-time, t_{OFF} = off-time of the switching period; t_S = 1/frequency

t_{OFF} must be greater than 400ns, or $t_S - t_{ON} > 400ns$.

$t_{ON} = DC \bullet t_S$

1MHz frequency or 1μs period is chosen for 12V to 5V.

$t_{ON} = 0.41 \bullet 1\mu s \cong 410ns$

$t_{OFF} = 1\mu s - 410ns \cong 590ns$

t_{ON} and t_{OFF} are above the minimums with adequate guard band.

Using the frequency = $(I_{ON}/[2.4V \bullet 10pF]) \bullet DC$, solve for $I_{ON} = (1MHz \bullet 2.4V \bullet 10pF) \bullet (1/0.41) \cong 58\mu A$. I_{ON} current calculated from 12V input was 103μA, so a resistor from f_{ADJ} to ground = (0.7V/15k) = 46μA. 103μA – 46μA = 57μA, sets the adequate I_{ON} current for proper frequency range for the higher duty cycle conversion of 12V to 5V. Input voltage range is limited to 9V to 16V. Higher input voltages can be used without the 15k on f_{ADJ}. The inductor ripple current gets too high above 16V, and the 400ns minimum off-time is limited below 9V.

APPLICATIONS INFORMATION

Equations for setting frequency for 5V to 3.3V:

$I_{ON} = (V_{IN} – 0.7V)/110k$; $I_{ON} = 39\mu A$

frequency = $(I_{ON}/[2.4V \bullet 10pF]) \bullet DC = 1.07MHz$; DC = duty cycle, duty cycle is (V_{OUT}/V_{IN})

$t_S = t_{ON} + t_{OFF}$, t_{ON} = on-time, t_{OFF} = off-time of the switching period; t_S = 1/frequency

t_{OFF} must be greater than 400ns, or $t_S – t_{ON} > 400ns$.

$t_{ON} = DC \bullet t_S$

~450kHz frequency or 2.22µs period is chosen for 5V to 3.3V. Frequency range is about 450kHz to 650kHz from 4.5V to 7V input.

$t_{ON} = 0.66 \bullet 2.22\mu s \cong 1.46\mu s$

$t_{OFF} = 2.22\mu s – 1.46\mu s \cong 760ns$

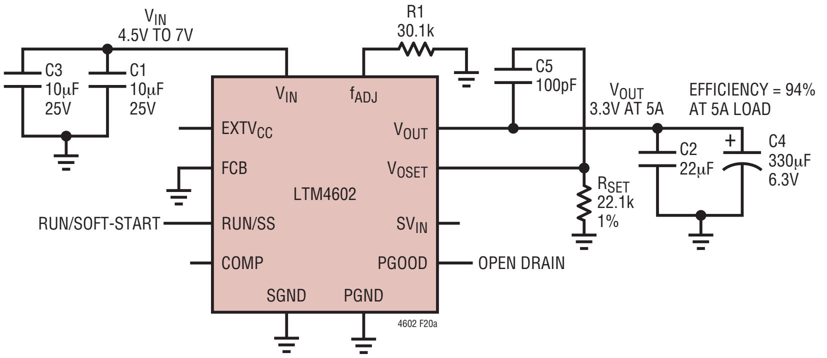
t_{ON} and t_{OFF} are above the minimums with adequate guard band.

Using the frequency = $(I_{ON}/[2.4V \bullet 10pF]) \bullet DC$, solve for $I_{ON} = (450kHz \bullet 2.4V \bullet 10pF) \bullet (1/0.66) \cong 16\mu A$. I_{ON} current calculated from 5V input was 39µA, so a resistor from f_{ADJ} to ground = (0.7V/30.1k) = 23µA. 39µA – 23µA = 16µA, sets the adequate I_{ON} current for proper frequency range for the higher duty cycle conversion of 5V to 3.3V. Input voltage range is limited to 4.5V to 7V. Higher input voltages can be used without the 30.1k on f_{ADJ}. The inductor ripple current gets too high above 7V, and the 400ns minimum off-time is limited below 4.5V.

In 12V to 3.3V applications, if a 35k resistor is added from the f_{ADJ} pin to ground, then a 2% efficiency gain will be achieved as shown in the 12V efficiency graph in the Typical Performance Characteristics. This is due to the lower transition losses in the power MOSFETs after lowering the switching frequency down from 1.3MHz to 950kHz.

APPLICATIONS INFORMATION

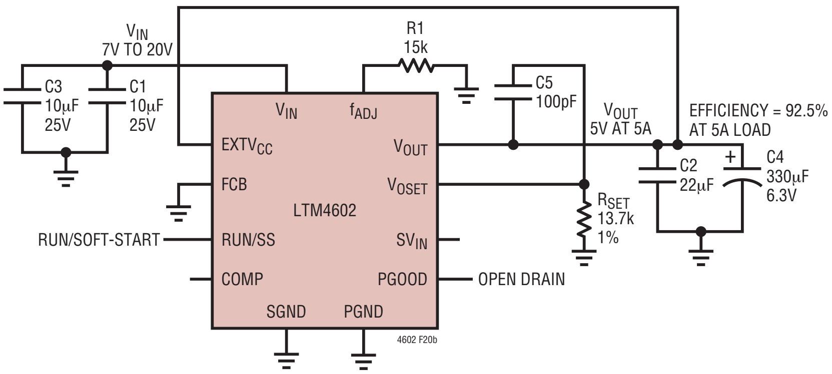
5V to 3.3V at 5A



5V TO 3.3V AT 5A WITH f_{ADJ} = 30.1k

C1, C3: TDK C3216X5R1E106MT
C2: TAIYO YUDEN, JMK316BJ226ML
C4: SANYO POSCAP, 6TPE330MIL

12V to 5V at 5A



7V TO 20V AT 5A WITH f_{ADJ} = 15k

C1, C3: TDK C3216X5R1E106MT
C2: TAIYO YUDEN, JMK316BJ226ML
C4: SANYO POSCAP, 6TPE330MIL

Figure 20. V_{IN} to V_{OUT} Step-Down Ratio for $12V_{IN}$ to $5V_{OUT}$ and $5V_{IN}$ to $3.3V_{OUT}$

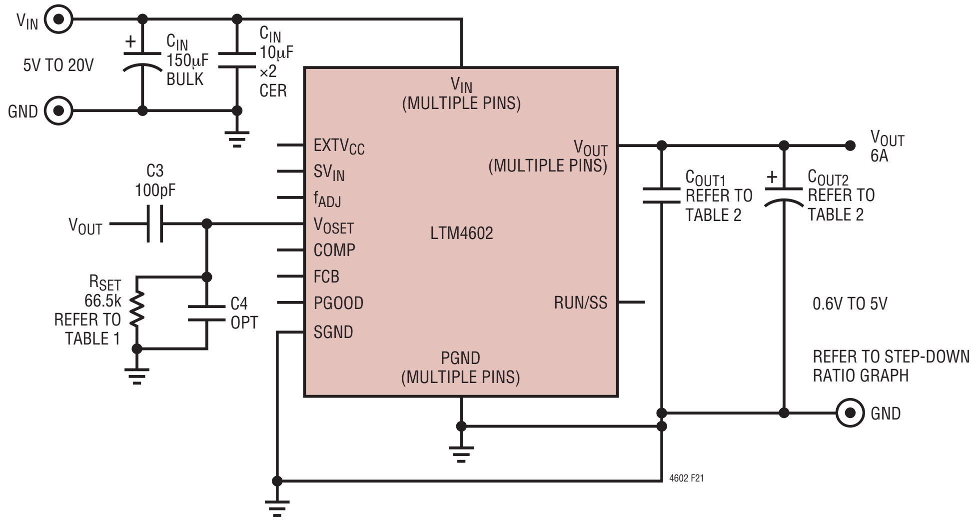
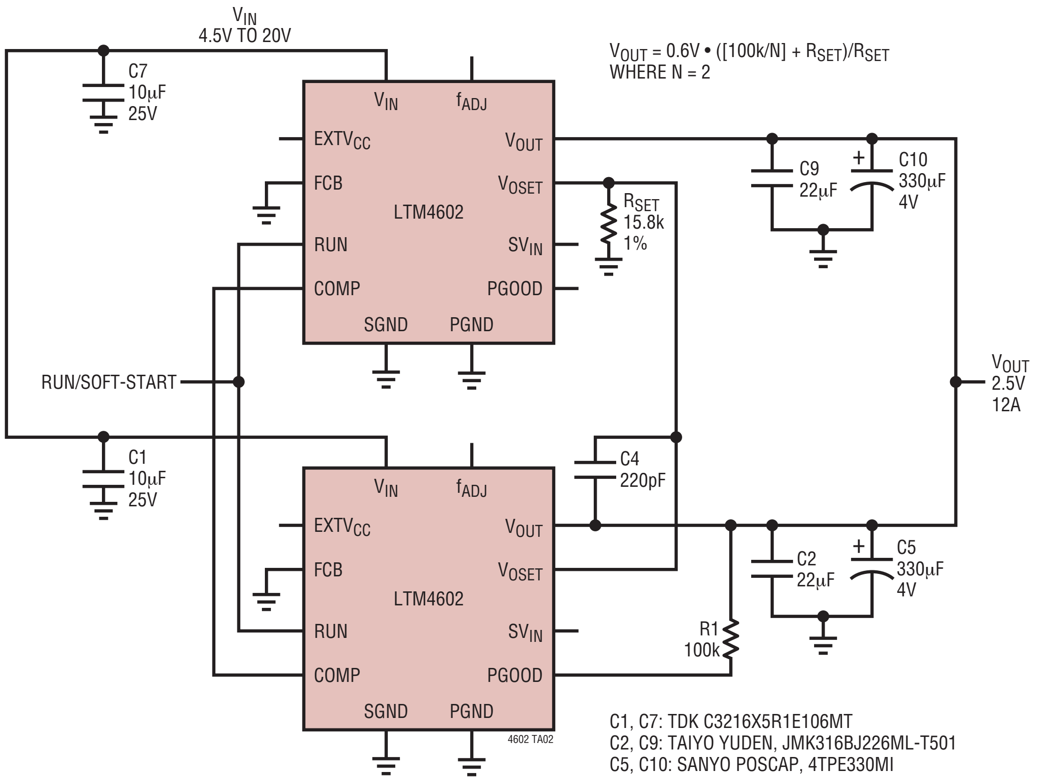


Figure 21. Typical Application, 5V to 20V Input, 0.6V to 5V Output, 6A Max

TYPICAL APPLICATION

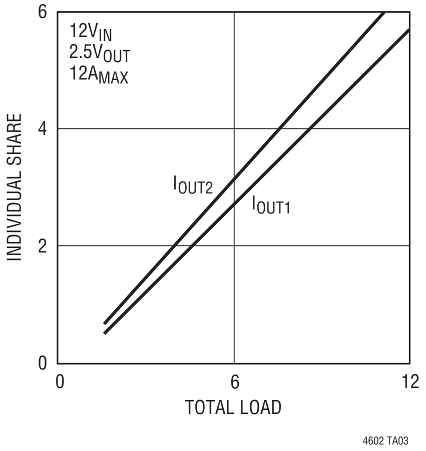
Parallel Operation and Load Sharing



$V_{OUT} = 0.6V \bullet ([100k/N] + R_{SET})/R_{SET}$
WHERE N = 2

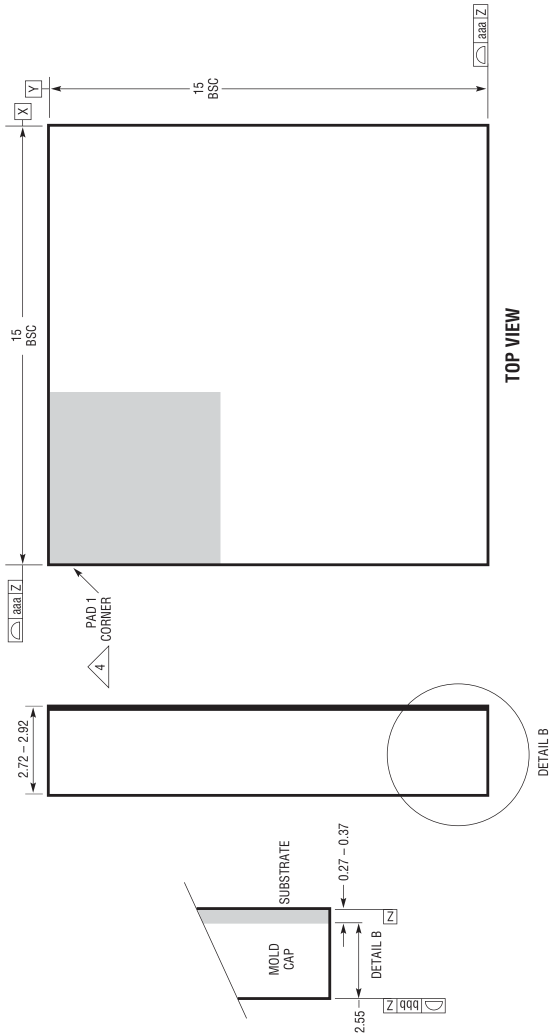
C1, C7: TDK C3216X5R1E106MT
C2, C9: TAIYO YUDEN, JMK316BJ226ML-T501
C5, C10: SANYO POSCAP, 4TPE330MI

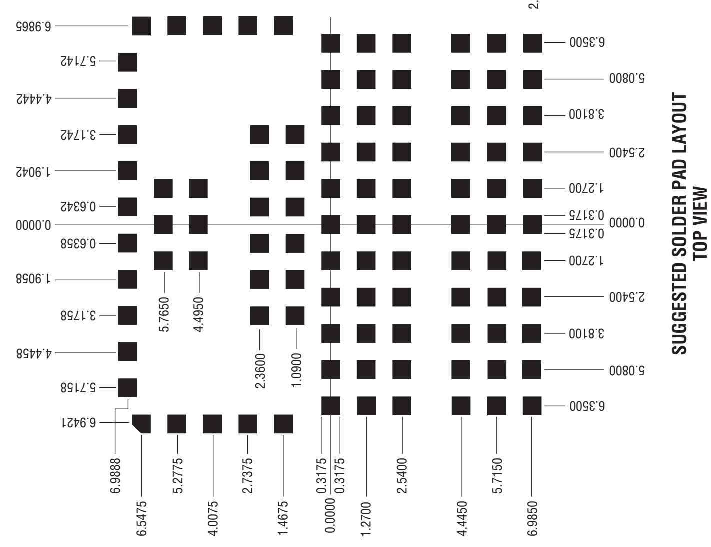
Current Sharing Between Two LTM4602 Modules



PACKAGE DESCRIPTION

LGA Package
104-Lead (15mm × 15mm)
(Reference LTM DWG # 05-05-1800)





NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994

2. ALL DIMENSIONS ARE IN MILLIMETERS

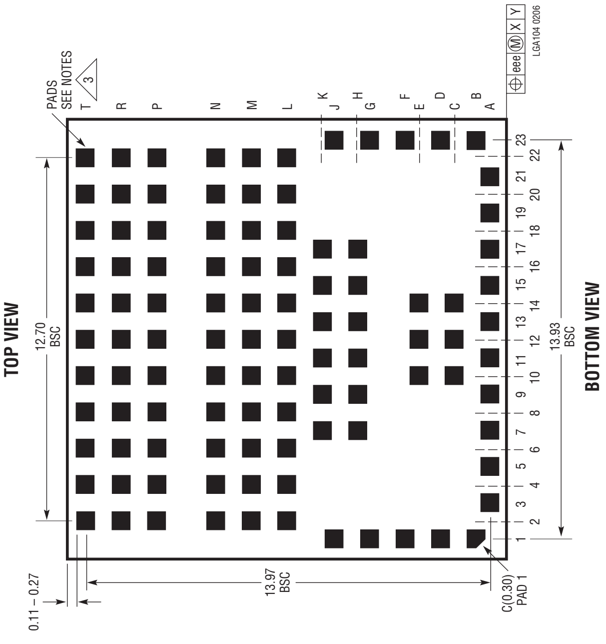
3 LAND DESIGNATION PER JESD MO-222, SPP-010

4 DETAILS OF PAD #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE PAD #1 IDENTIFIER IS A MARKED FEATURE OR A NOTCHED BEVELED PAD

5. PRIMARY DATUM -Z- IS SEATING PLANE

6. THE TOTAL NUMBER OF PADS: 104

SYMBOL	TOLERANCE
aaa	0.15
bbb	0.10
eee	0.15



PACKAGE DESCRIPTION

Pin Assignment Tables
(Arranged by Pin Number)

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
A1	-	B1	V_{IN}	C1	-	D1	V_{IN}	E1	-	F1	V_{IN}	G1	PGND	H1	-
A2	-	B2	-	C2	-	D2	-	E2	-	F2	-	G2	-	H2	-
A3	V_{IN}	B3	-	C3	-	D3	-	E3	-	F3	-	G3	-	H3	-
A4	-	B4	-	C4	-	D4	-	E4	-	F4	-	G4	-	H4	-
A5	V_{IN}	B5	-	C5	-	D5	-	E5	-	F5	-	G5	-	H5	-
A6	-	B6	-	C6	-	D6	-	E6	-	F6	-	G6	-	H6	-
A7	V_{IN}	B7	-	C7	-	D7	-	E7	-	F7	-	G7	-	H7	PGND
A8	-	B8	-	C8	-	D8	-	E8	-	F8	-	G8	-	H8	-
A9	V_{IN}	B9	-	C9	-	D9	-	E9	-	F9	-	G9	-	H9	PGND
A10	-	B10	-	C10	V_{IN}	D10	-	E10	V_{IN}	F10	-	G10	-	H10	-
A11	V_{IN}	B11	-	C11	-	D11	-	E11	-	F11	-	G11	-	H11	PGND
A12	-	B12	-	C12	V_{IN}	D12	-	E12	V_{IN}	F12	-	G12	-	H12	-
A13	V_{IN}	B13	-	C13	-	D13	-	E13	-	F13	-	G13	-	H13	PGND
A14	-	B14	-	C14	V_{IN}	D14	-	E14	V_{IN}	F14	-	G14	-	H14	-
A15	f_{ADJ}	B15	-	C15	-	D15	-	E15	-	F15	-	G15	-	H15	PGND
A16	-	B16	-	C16	-	D16	-	E16	-	F16	-	G16	-	H16	-
A17	SV_{IN}	B17	-	C17	-	D17	-	E17	-	F17	-	G17	-	H17	PGND
A18	-	B18	-	C18	-	D18	-	E18	-	F18	-	G18	-	H18	-
A19	$EXTV_{CC}$	B19	-	C19	-	D19	-	E19	-	F19	-	G19	-	H19	-
A20	-	B20	-	C20	-	D20	-	E20	-	F20	-	G20	-	H20	-
A21	V_{OSET}	B21	-	C21	-	D21	-	E21	-	F21	-	G21	-	H21	-
A22	-	B22	-	C22	-	D22	-	E22	-	F22	-	G22	-	H22	-
A23	-	B23	COMP	C23	-	D23	SGND	E23	-	F23	RUN/SS	G23	FCB	H23	-

PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME	PIN	NAME
J1	PGND	K1	-	L1	-	M1	-	N1	-	P1	-	R1	-	T1	-
J2	-	K2	-	L2	PGND	M2	PGND	N2	PGND	P2	V_{OUT}	R2	V_{OUT}	T2	V_{OUT}
J3	-	K3	-	L3	-	M3	-	N3	-	P3	-	R3	-	T3	-
J4	-	K4	-	L4	PGND	M4	PGND	N4	PGND	P4	V_{OUT}	R4	V_{OUT}	T4	V_{OUT}
J5	-	K5	-	L5	-	M5	-	N5	-	P5	-	R5	-	T5	-
J6	-	K6	-	L6	PGND	M6	PGND	N6	PGND	P6	V_{OUT}	R6	V_{OUT}	T6	V_{OUT}
J7	-	K7	PGND	L7	-	M7	-	N7	-	P7	-	R7	-	T7	-
J8	-	K8		L8	PGND	M8	PGND	N8	PGND	P8	V_{OUT}	R8	V_{OUT}	T8	V_{OUT}
J9	-	K9	PGND	L9	-	M9	-	N9	-	P9	-	R9	-	T9	-
J10	-	K10		L10	PGND	M10	PGND	N10	PGND	P10	V_{OUT}	R10	V_{OUT}	T10	V_{OUT}
J11	-	K11	PGND	L11	-	M11	-	N11	-	P11	-	R11	-	T11	-
J12	-	K12	-	L12	PGND	M12	PGND	N12	PGND	P12	V_{OUT}	R12	V_{OUT}	T12	V_{OUT}
J13	-	K13	PGND	L13	-	M13	-	N13	-	P13	-	R13	-	T13	-
J14	-	K14	-	L14	PGND	M14	PGND	N14	PGND	P14	V_{OUT}	R14	V_{OUT}	T14	V_{OUT}
J15	-	K15	PGND	L15	-	M15	-	N15	-	P15	-	R15	-	T15	-
J16	-	K16	-	L16	PGND	M16	PGND	N16	PGND	P16	V_{OUT}	R16	V_{OUT}	T16	V_{OUT}
J17	-	K17	PGND	L17	-	M17	-	N17	-	P17	-	R17	-	T17	-
J18	-	K18	-	L18	PGND	M18	PGND	N18	PGND	P18	V_{OUT}	R18	V_{OUT}	T18	V_{OUT}
J19	-	K19	-	L19	-	M19	-	N19	-	P19	-	R19	-	T19	-
J20	-	K20	-	L20	PGND	M20	PGND	N20	PGND	P20	V_{OUT}	R20	V_{OUT}	T20	V_{OUT}
J21	-	K21	-	L21	-	M21	-	N21	-	P21	-	R21	-	T21	-
J22	-	K22	-	L22	PGND	M22	PGND	N22	PGND	P22	V_{OUT}	R22	V_{OUT}	T22	V_{OUT}
J23	PGOOD	K23	-	L23	-	M23	-	N23	-	P23	-	R23	-	T23	-

PACKAGE DESCRIPTION

Pin Assignment Tables
(Arranged by Pin Number)

PIN	NAME
G1	PGND
H7	PGND
H9	PGND
H11	PGND
H13	PGND
H15	PGND
H17	PGND
J1	PGND
K7	PGND
K9	PGND
K11	PGND
K13	PGND
K15	PGND
K17	PGND
L2	PGND
L4	PGND
L6	PGND
L8	PGND
L10	PGND
L12	PGND
L14	PGND
L16	PGND
L18	PGND
L20	PGND
L22	PGND
M2	PGND
M4	PGND
M6	PGND
M8	PGND
M10	PGND
M12	PGND
M14	PGND
M16	PGND
M18	PGND
M20	PGND
M22	PGND
N2	PGND
N4	PGND
N6	PGND
N8	PGND
N10	PGND
N12	PGND
N14	PGND
N16	PGND
N18	PGND
N20	PGND
N22	PGND

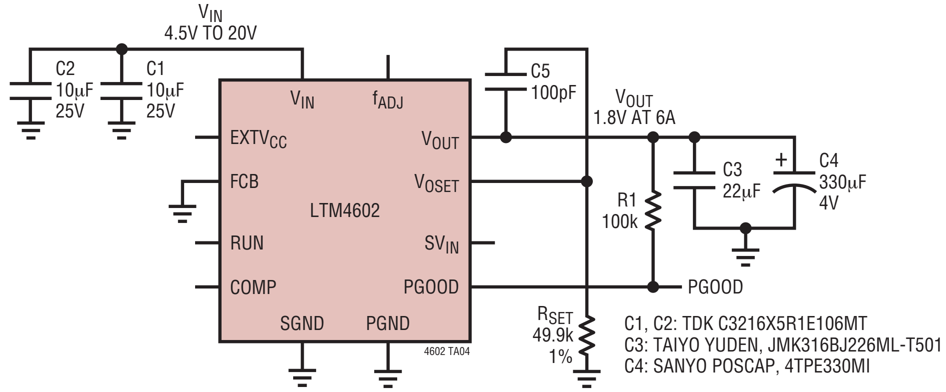
PIN	NAME
P2	V_{OUT}
P4	V_{OUT}
P6	V_{OUT}
P8	V_{OUT}
P10	V_{OUT}
P12	V_{OUT}
P14	V_{OUT}
P16	V_{OUT}
P18	V_{OUT}
P20	V_{OUT}
P22	V_{OUT}
R2	V_{OUT}
R4	V_{OUT}
R6	V_{OUT}
R8	V_{OUT}
R10	V_{OUT}
R12	V_{OUT}
R14	V_{OUT}
R16	V_{OUT}
R18	V_{OUT}
R20	V_{OUT}
R22	V_{OUT}
T2	V_{OUT}
T4	V_{OUT}
T6	V_{OUT}
T8	V_{OUT}
T10	V_{OUT}
T12	V_{OUT}
T14	V_{OUT}
T16	V_{OUT}
T18	V_{OUT}
T20	V_{OUT}
T22	V_{OUT}

PIN	NAME
A3	V_{IN}
A5	V_{IN}
A7	V_{IN}
A9	V_{IN}
A11	V_{IN}
A13	V_{IN}
B1	V_{IN}
C10	V_{IN}
C12	V_{IN}
C14	V_{IN}
D1	V_{IN}
E10	V_{IN}
E12	V_{IN}
E14	V_{IN}
F1	V_{IN}

PIN	NAME
A15	f_{ADJ}
A17	SV_{IN}
A19	$EXTV_{CC}$
A21	V_{OSET}
B23	COMP
D23	SGND
F23	RUN/SS
G23	FCB
J23	PGOOD

TYPICAL APPLICATION

1.8V, 6A Regulator



C1, C2: TDK C3216X5R1E106MT
C3: TAIYO YUDEN, JMK316BJ226ML-T501
C4: SANYO POSCAP, 4TPE330MI

RELATED PARTS

PART NUMBER	DESCRIPTION	COMMENTS
LTC2900	Quad Supply Monitor with Adjustable Reset Timer	Monitors Four Supplies; Adjustable Reset Timer
LTC2923	Power Supply Tracking Controller	Tracks Both Up and Down; Power Supply Sequencing
LT3825/LT3837	Synchronous Isolated Flyback Controllers	No Optocoupler Required; 3.3V, 12A Output; Simple Design
LTM4600	10A DC/DC μModule	10A Basic DC/DC Module
LTM4601	12A DC/DC μModule with PLL, Output Tracking/ Margining and Remote Sensing	Synchronizable, PolyPhase® Operation, LTM4601-1 Version has no Remote Sensing, Fast Transient Response
LTM4603	6A DC/DC μModule with PLL and Output Tracking/ Margining and Remote Sensing	Synchronizable, PolyPhase Operation, LTM4603-1 Version has no Remote Sensing, Fast Transient Response

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