MCP6561/1R/1U/2/4

1.8V Low-Power Push-Pull Output Comparator

Features

- Propagation Delay at 1.8V_{DD}:
  - 56 ns (typical) High-to-Low
  - 49 ns (typical) Low-to-High
- Low Quiescent Current: 100 µA (typical)
- Input Offset Voltage: ±3 mV (typical)
- Rail-to-Rail Input: V_{SS} - 0.3V to V_{DD} + 0.3V
- CMOS/TTL-Compatible Output
- Wide Supply Voltage Range: 1.8V to 5.5V
- Available in Single, Dual, and Quad
- Packages: SC70-5, SOT-23-5, SOIC, MSOP, TSSOP

Typical Applications

- Laptop Computers
- Mobile Phones
- Hand-held Electronics
- RC Timers
- Alarm and Monitoring Circuits
- Window Comparators
- Multivibrators

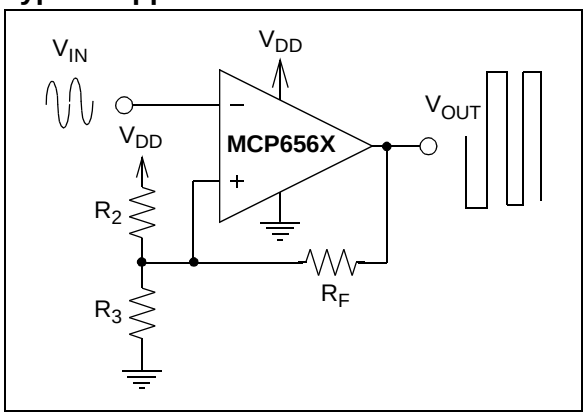
Design Aids

- Microchip Advanced Part Selector (MAPS)
- Analog Demonstration and Evaluation Boards
- Application Notes

Related Devices

- Open-Drain Output: MCP6566/6R/6U/7/9

Typical Application



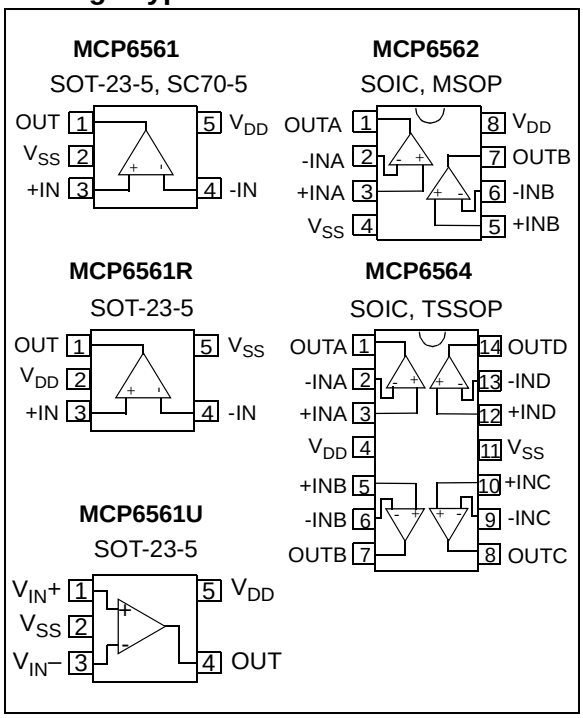
Description

The Microchip Technology, Inc. MCP6561/1R/1U/2/4 families of CMOS/TTL compatible comparators are offered in single, dual, and quad configurations.

These comparators are optimized for low power 1.8V, single-supply applications with greater than rail-to-rail input operation. The internal input hysteresis eliminates output switching due to internal input noise voltage, reducing current draw. The push-pull output of the MCP6561/1R/1U/2/4 family supports rail-to-rail output swing, and interfaces with CMOS/TTL logic. The output toggle frequency can reach a typical of 4 MHz (typical) while limiting supply current surges and dynamic power consumption during switching.

This family operates with single supply voltage of 1.8V to 5.5V while drawing less than 100 µA/comparator of quiescent current (typical).

Package Types



NOTES:

1.0 ELECTRICAL CHARACTERISTICS

1.1 Maximum Ratings †

V_{DD} - V_{SS} 6.5V
Analog Input (V_{IN}) †† .....V_{SS} - 1.0V to V_{DD} + 1.0V
All other inputs and outputs.....V_{SS} - 0.3V to V_{DD} + 0.3V
Difference Input voltage .....|V_{DD} - V_{SS}|
Output Short Circuit Current ..... ±25 mA
Current at Input Pins ..... ±2 mA
Current at Output and Supply Pins ..... ±50 mA
Storage temperature ..... -65°C to +150°C
Ambient temp. with power applied ..... -40°C to +125°C
Junction temp..... +150°C
ESD protection on all pins (HBM/MM).....≥ 4 kV/300V

† **Notice:** Stresses above those listed under “Maximum Ratings” may cause permanent damage to the device. This is a stress rating only and functional operation of the device at those or any other conditions above those indicated in the operational listings of this specification is not implied. Exposure to maximum rating conditions for extended periods may affect device reliability.

†† See **Section 4.1.2 “Input Voltage and Current Limits”**

DC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated: V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}- = V_{SS}, R_L = 10 kΩ to V_{DD}/2 (see Figure 1-1).

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Power Supply						
Supply Voltage	V_{DD}	1.8	—	5.5	V	
Quiescent Current per comparator	I_Q	60	100	130	µA	I_{OUT} = 0
Power Supply Rejection Ratio	PSRR	63	70	—	dB	V_{CM} = V_{SS}
Input						
Input Offset Voltage	V_{OS}	-10	±3	+10	mV	V_{CM} = V_{SS} **(Note 1)**
Input Offset Drift	$\Delta V_{OS}/\Delta T$	—	±2	—	µV/°C	V_{CM} = V_{SS}
Input Offset Current	I_{OS}	—	±1	—	pA	V_{CM} = V_{SS}
Input Bias Current	I_B	—	1	—	pA	T_A = +25°C, V_{IN}- = V_{DD}/2
		—	60	—	pA	T_A = +85°C, V_{IN}- = V_{DD}/2
		—	1500	5000	pA	T_A = +125°C, V_{IN}- = V_{DD}/2
Input Hysteresis Voltage	V_{HYST}	1.0	—	5.0	mV	V_{CM} = V_{SS} **(Notes 1, 2)**
Input Hysteresis Linear Temp. Co.	TC_1	—	10	—	µV/°C	
Input Hysteresis Quadratic Temp. Co.	TC_2	—	0.3	—	µV/°C^2	
Common-mode Input Voltage Range	V_{CMR}	V_{SS}–0.2	—	V_{DD}+0.2	V	V_{DD} = 1.8V
		V_{SS}–0.3	—	V_{DD}+0.3	V	V_{DD} = 5.5V
Common-mode Rejection Ratio	CMRR	54	66	—	dB	V_{CM}= -0.3V to V_{DD}+0.3V, V_{DD} = 5.5V
		50	63	—	dB	V_{CM}= V_{DD}/2 to V_{DD}+0.3V, V_{DD} = 5.5V
		54	65	—	dB	V_{CM}= -0.3V to V_{DD}/2, V_{DD} = 5.5V
Common-mode Input Impedance	Z_{CM}	—	10^{13}||4	—	Ω||pF	
Differential Input Impedance	Z_{DIFF}	—	10^{13}||2	—	Ω||pF	
Push-Pull Output						
High-Level Output Voltage	V_{OH}	V_{DD}–0.7	—	—	V	I_{OUT} = -3 mA/-8 mA with V_{DD} = 1.8V/5.5V **(Note 3)**
Low-Level Output Voltage	V_{OL}	—	—	0.6	V	I_{OUT} = 3 mA/8 mA with V_{DD} = 1.8V/5.5V **(Note 3)**
Short Circuit Current	I_{SC}	—	±30	—	mA	**Note 3**
Output Pin Capacitance	C_{OUT}	—	8	—	pF	

Note 1: The input offset voltage is the center of the input-referred trip points. The input hysteresis is the difference between the input-referred trip points.

2: V_{HYST} at different temperatures is estimated using V_{HYST} (T_A) = $V_{HYST\ @\ +25°C}$ + (T_A - 25°C) TC_1 + (T_A - 25°C)^2 TC_2.

3: Limit the output current to Absolute Maximum Rating of 50 mA.

AC CHARACTERISTICS

Electrical Characteristics: Unless otherwise indicated: V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}- = V_{SS}, R_L = 10 kΩ to V_{DD}/2, and C_L = 25 pF. (see Figure 1-1).

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Propagation Delay						
High-to-Low,100 mV Overdrive	t_{PHL}	—	56	80	ns	V_{CM}= V_{DD}/2, V_{DD} = 1.8V
		—	34	80	ns	V_{CM}= V_{DD}/2, V_{DD} = 5.5V
Low-to-High, 100 mV Overdrive	t_{PLH}	—	49	80	ns	V_{CM}= V_{DD}/2, V_{DD} = 1.8V
		—	47	80	ns	V_{CM}= V_{DD}/2, V_{DD} = 5.5V
Skew 1	t_{PDS}	—	±10	—	ns	
Output						
Rise Time	t_R	—	20	—	ns	
Fall Time	t_F	—	20	—	ns	
Maximum Toggle Frequency	f_{TG}	—	4	—	MHz	V_{DD} = 5.5V
		—	2	—	MHz	V_{DD} = 1.8V
Input Voltage Noise 2	E_{NI}	—	350	—	μV_{P-P}	10 Hz to 10 MHz

Note 1: Propagation Delay Skew is defined as: $t_{PDS} = t_{PLH} - t_{PHL}$.

2: ENI is based on SPICE simulation.

TEMPERATURE SPECIFICATIONS

Electrical Characteristics: Unless otherwise indicated: V_{DD} = +1.8V to +5.5V and V_{SS} = GND.

Parameters	Symbol	Min	Typ	Max	Units	Conditions
Temperature Ranges						
Specified Temperature Range	T_A	-40	—	+125	°C	
Operating Temperature Range	T_A	-40	—	+125	°C	
Storage Temperature Range	T_A	-65	—	+150	°C	
Thermal Package Resistances						
Thermal Resistance, SC70-5	θ_{JA}	—	331	—	°C/W	
Thermal Resistance, SOT-23-5	θ_{JA}	—	220.7	—	°C/W	
Thermal Resistance, 8L-SOIC	θ_{JA}	—	149.5	—	°C/W	
Thermal Resistance, 8L-MSOP	θ_{JA}	—	211	—	°C/W	
Thermal Resistance, 14L-SOIC	θ_{JA}	—	95.3	—	°C/W	
Thermal Resistance, 14L-TSSOP	θ_{JA}	—	100	—	°C/W	

1.2 Test Circuit Configuration

This test circuit configuration is used to determine the AC and DC specifications.

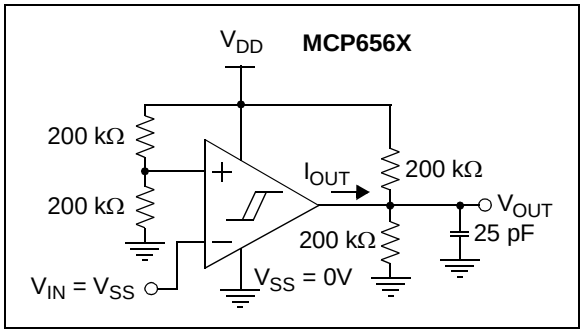


FIGURE 1-1: *AC and DC Test Circuit for the Push-Pull Output Comparators.*

2.0 TYPICAL PERFORMANCE CURVES

Note: The graphs and tables provided following this note are a statistical summary based on a limited number of samples and are provided for informational purposes only. The performance characteristics listed herein are not tested or guaranteed. In some graphs or tables, the data presented may be outside the specified operating range (e.g., outside specified power supply range) and therefore outside the warranted range.

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 10 kΩ to $V_{DD}/2$, and C_L = 25 pF.

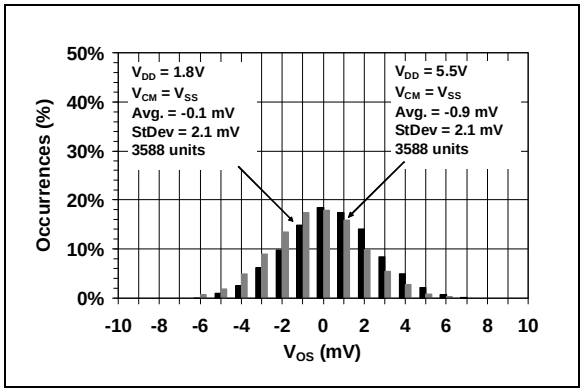


FIGURE 2-1: *Input Offset Voltage.*

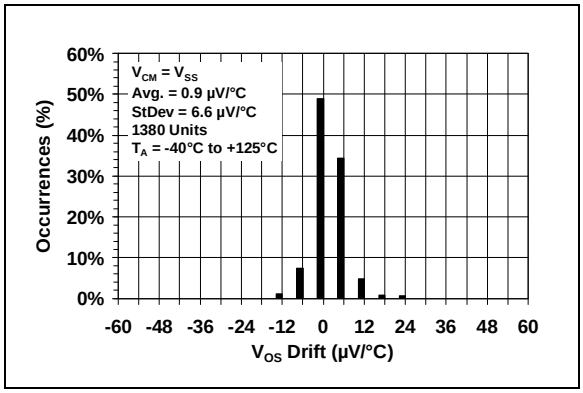


FIGURE 2-2: *Input Offset Voltage Drift.*

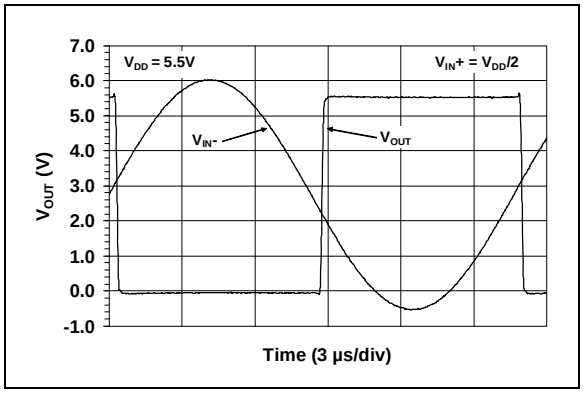


FIGURE 2-3: *Input vs. Output Signal, No Phase Reversal.*

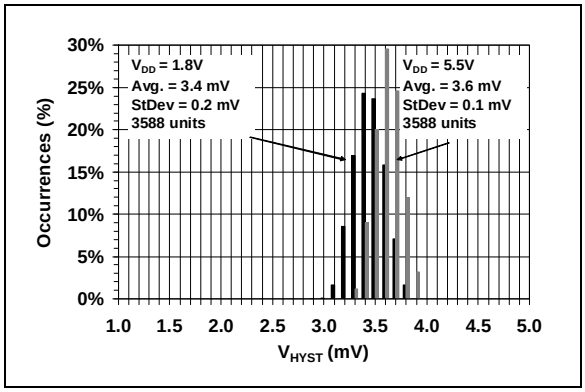


FIGURE 2-4: *Input Hysteresis Voltage.*

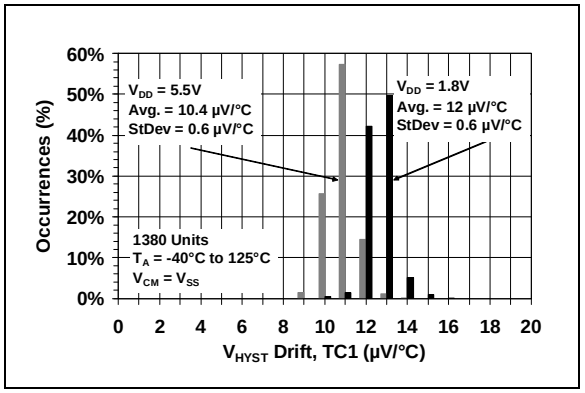


FIGURE 2-5: *Input Hysteresis Voltage Drift - Linear Temp. Co. (TC1).*

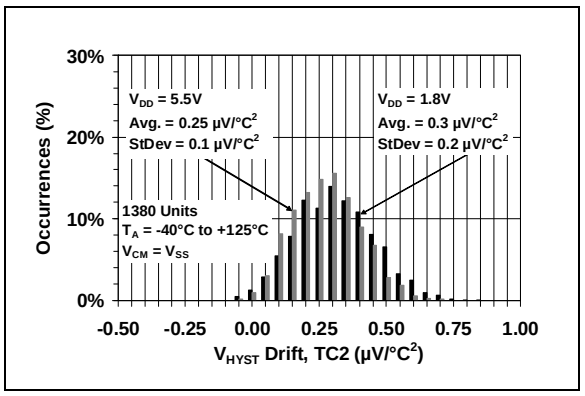


FIGURE 2-6: *Input Hysteresis Voltage Drift - Quadratic Temp. Co. (TC2).*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 10 kΩ to $V_{DD}/2$, and C_L = 25 pF.

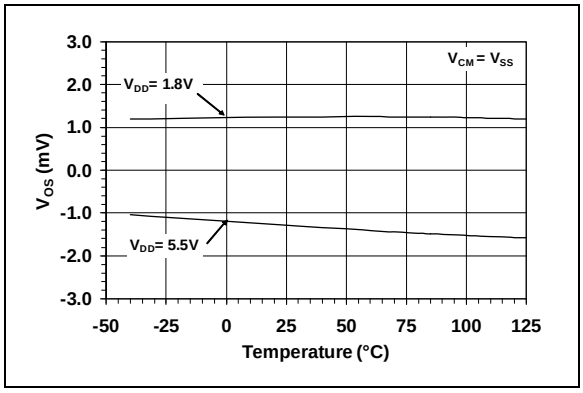


FIGURE 2-7: *Input Offset Voltage vs. Temperature.*

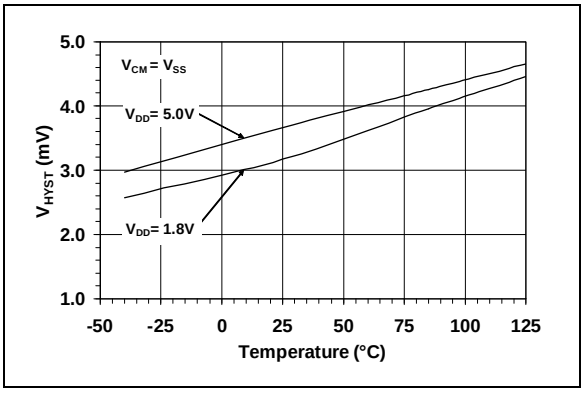


FIGURE 2-10: *Input Hysteresis Voltage vs. Temperature.*

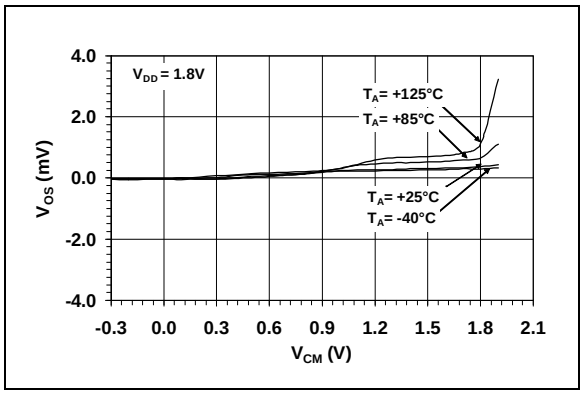


FIGURE 2-8: *Input Offset Voltage vs. Common-mode Input Voltage.*

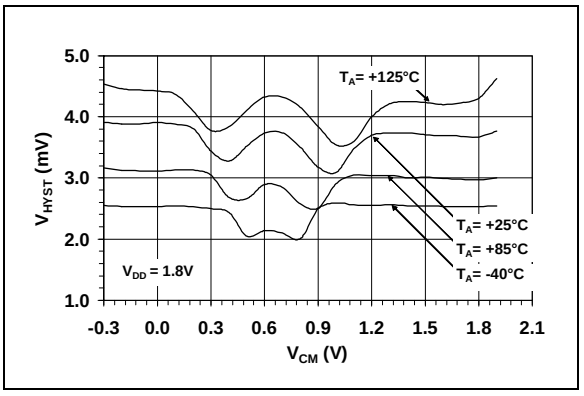


FIGURE 2-11: *Input Hysteresis Voltage vs. Common-mode Input Voltage.*

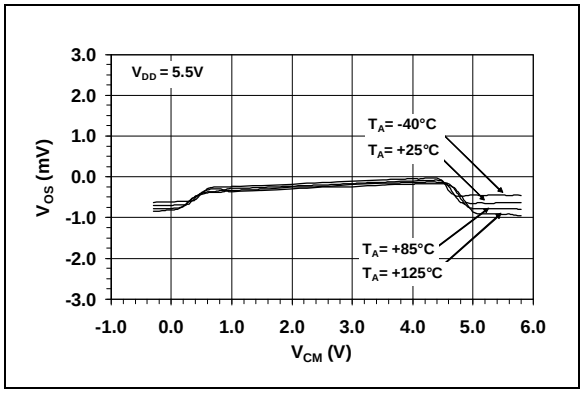


FIGURE 2-9: *Input Offset Voltage vs. Common-mode Input Voltage.*

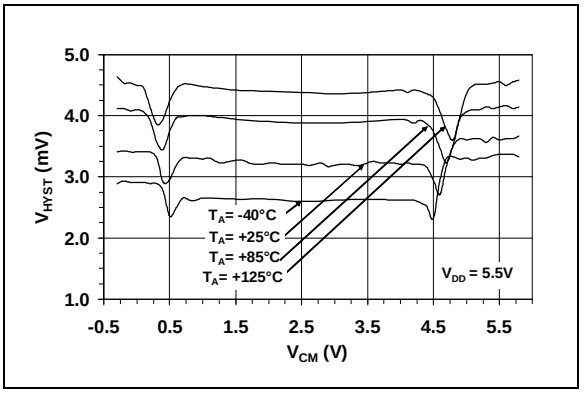


FIGURE 2-12: *Input Hysteresis Voltage vs. Common-mode Input Voltage.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_L = 10 kΩ to V_{DD}/2, and C_L = 25 pF.

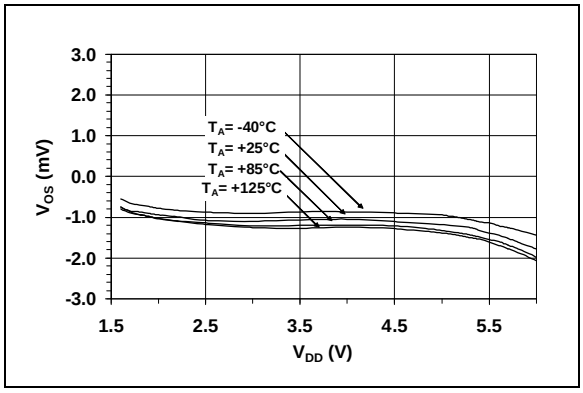


FIGURE 2-13: *Input Offset Voltage vs. Supply Voltage vs. Temperature.*

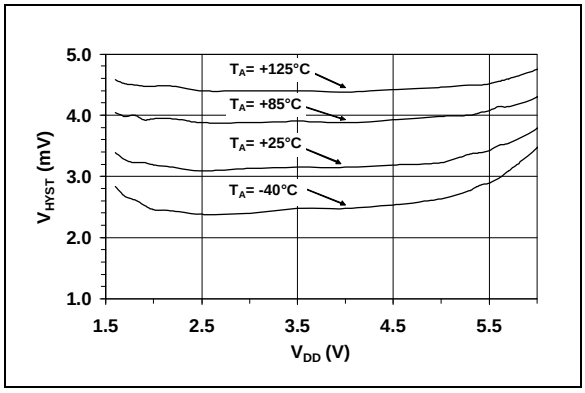


FIGURE 2-16: *Input Hysteresis Voltage vs. Supply Voltage vs. Temperature.*

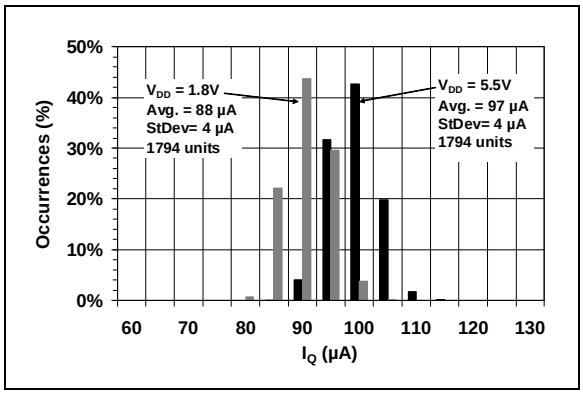


FIGURE 2-14: *Quiescent Current.*

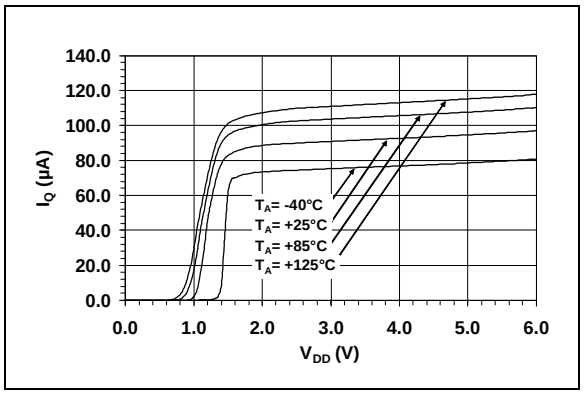


FIGURE 2-17: *Quiescent Current vs. Supply Voltage vs Temperature.*

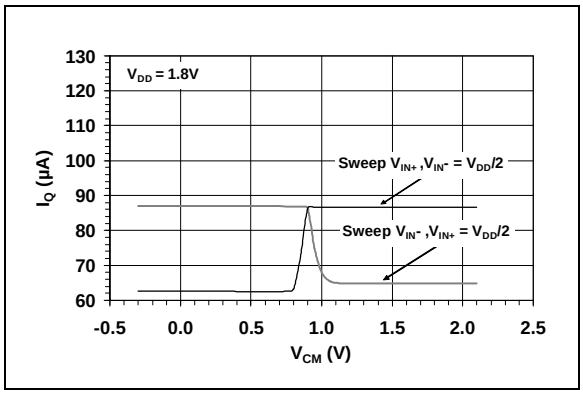


FIGURE 2-15: *Quiescent Current vs. Common-mode Input Voltage.*

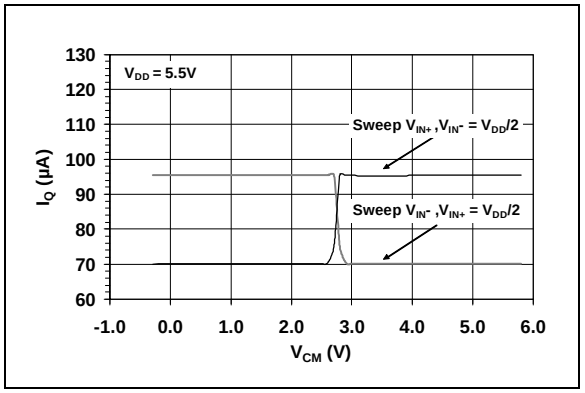


FIGURE 2-18: *Quiescent Current vs. Common-mode Input Voltage.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 10 kΩ to $V_{DD}/2$, and C_L = 25 pF.

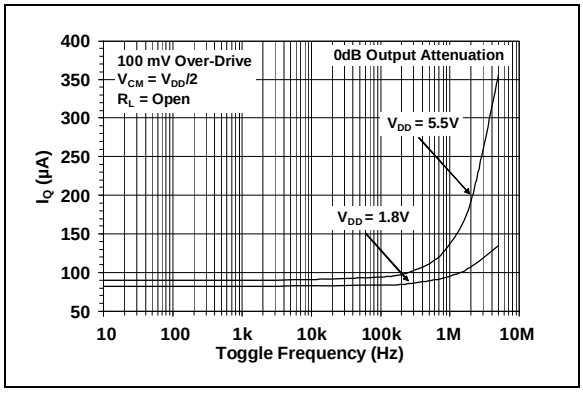


FIGURE 2-19: *Quiescent Current vs. Toggle Frequency.*

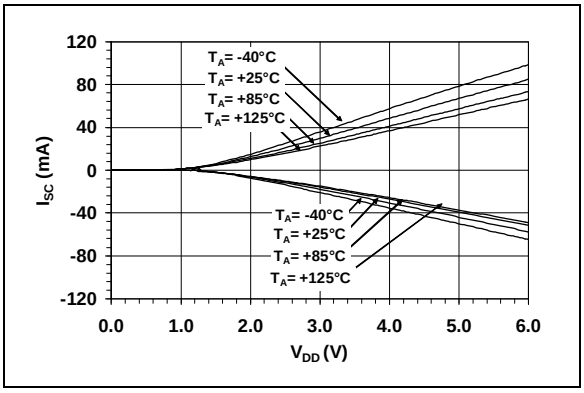


FIGURE 2-22: *Short Circuit Current vs. Supply Voltage vs. Temperature.*

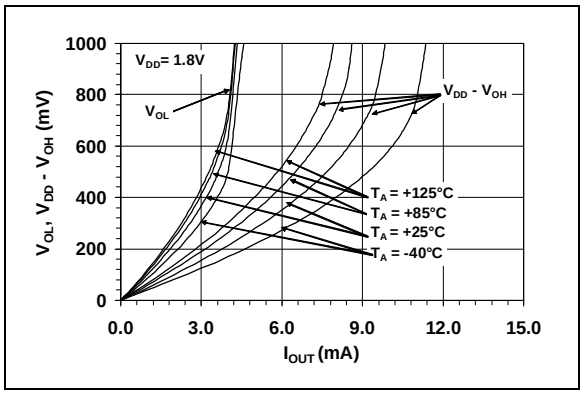


FIGURE 2-20: *Output Headroom vs. Output Current.*

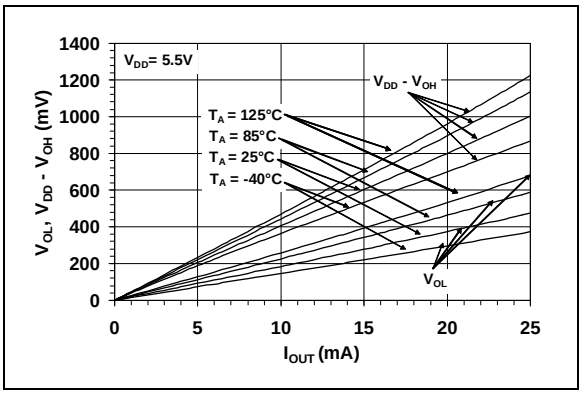


FIGURE 2-23: *Output Headroom vs.Output Current.*

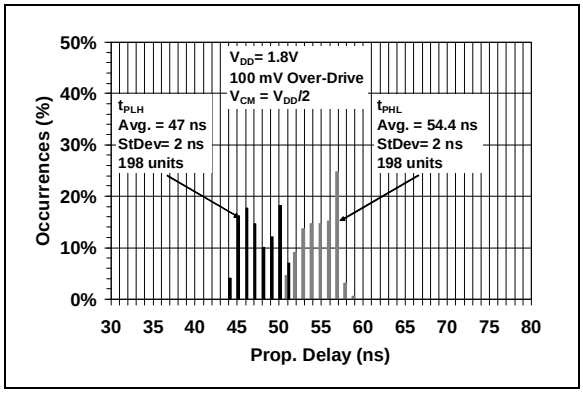


FIGURE 2-21: *Low-to-High and High-to-Low Propagation Delays.*

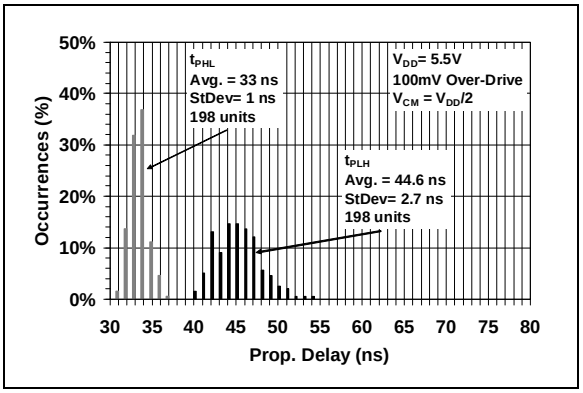


FIGURE 2-24: *Low-to-High and High-to-Low Propagation Delays .*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_L = 10 kΩ to V_{DD}/2, and C_L = 25 pF.

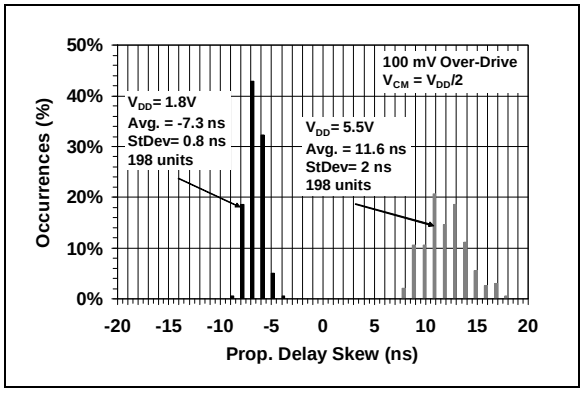


FIGURE 2-25: *Propagation Delay Skew.*

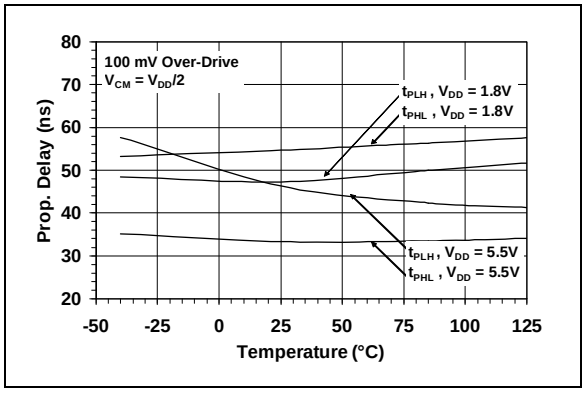


FIGURE 2-28: *Propagation Delay vs. Temperature.*

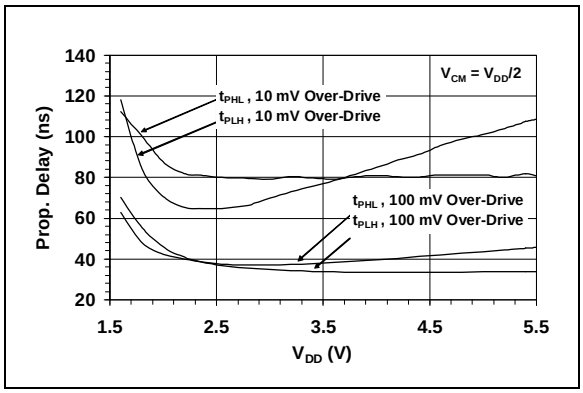


FIGURE 2-26: *Propagation Delay vs. Supply Voltage.*

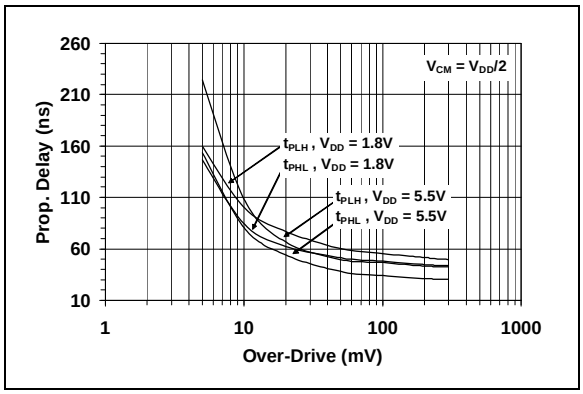


FIGURE 2-29: *Propagation Delay vs. Input Over-Drive.*

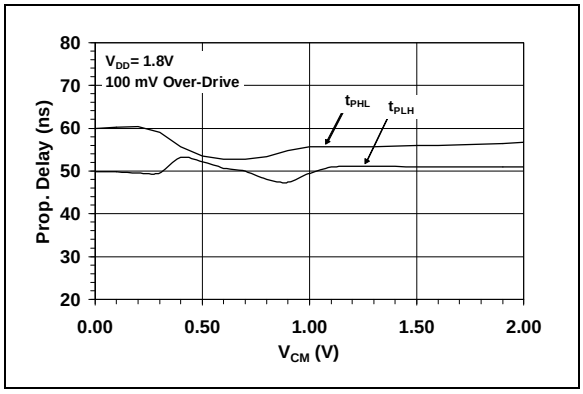


FIGURE 2-27: *Propagation Delay vs. Common-mode Input Voltage.*

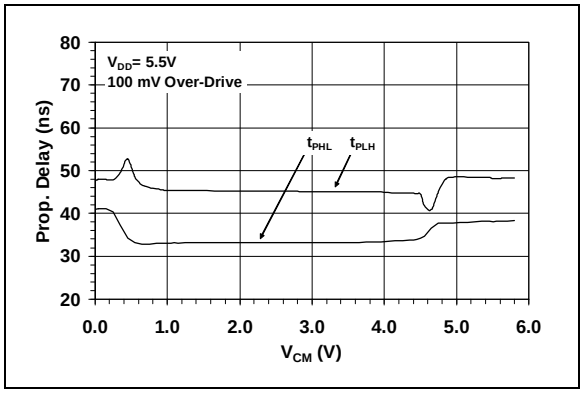


FIGURE 2-30: *Propagation Delay vs. Common-mode Input Voltage.*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, $V_{IN}+ = V_{DD}/2$, $V_{IN}-$ = GND, R_L = 10 kΩ to $V_{DD}/2$, and C_L = 25 pF.

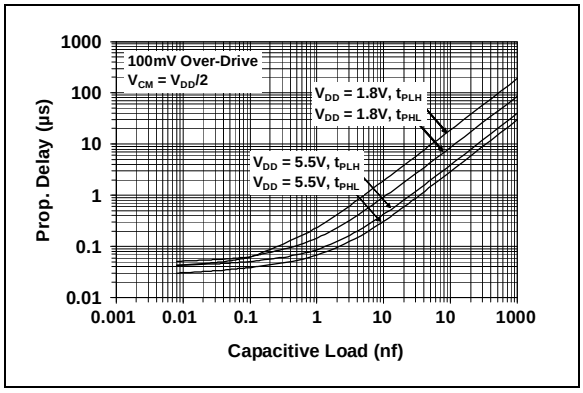


FIGURE 2-31: *Propagation Delay vs. Capacitive Load.*

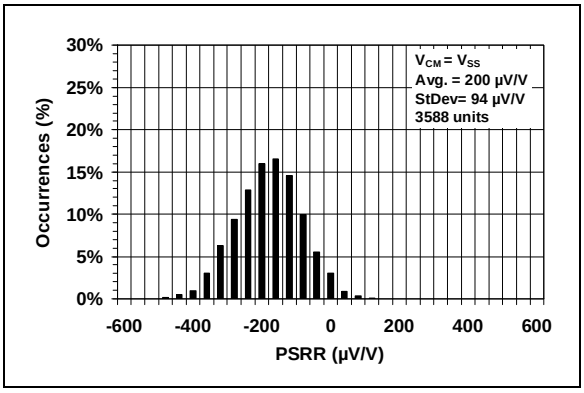


FIGURE 2-34: *Power Supply Rejection Ratio (PSRR).*

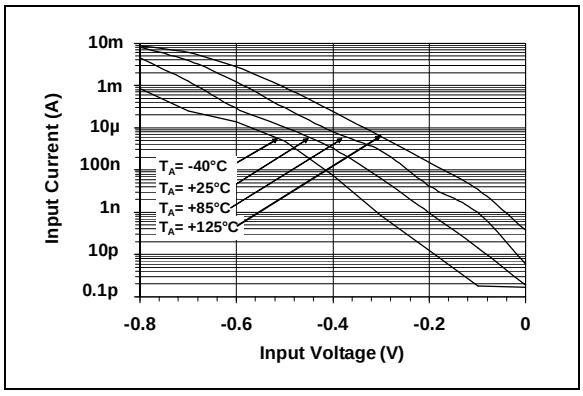


FIGURE 2-32: *Input Bias Current vs. Input Voltage vs Temperature.*

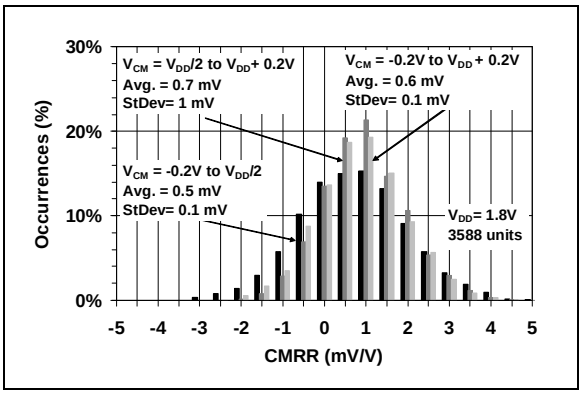


FIGURE 2-35: *Common-mode Rejection Ratio (CMRR).*

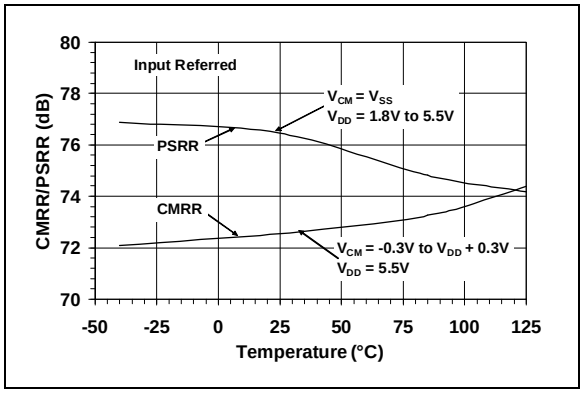


FIGURE 2-33: *Common-mode Rejection Ratio and Power Supply Rejection Ratio vs. Temperature.*

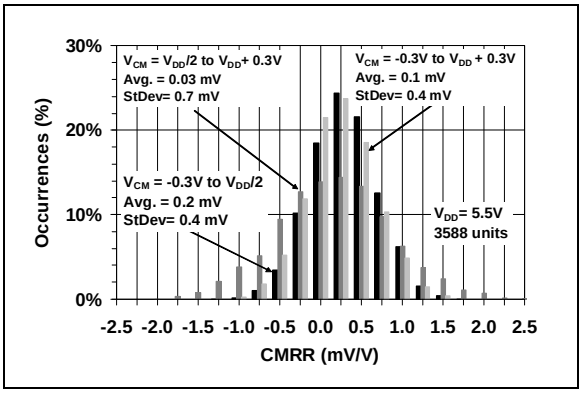


FIGURE 2-36: *Common-mode Rejection Ratio (CMRR).*

Note: Unless otherwise indicated, V_{DD} = +1.8V to +5.5V, V_{SS} = GND, T_A = +25°C, V_{IN}+ = V_{DD}/2, V_{IN}– = GND, R_L = 10 kΩ to V_{DD}/2, and C_L = 25 pF.

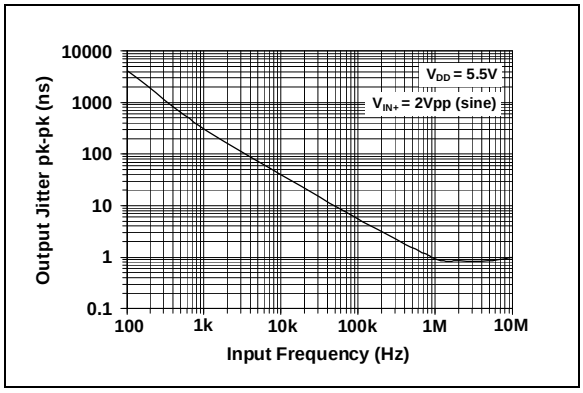


FIGURE 2-37: *Output Jitter vs. Input Frequency.*

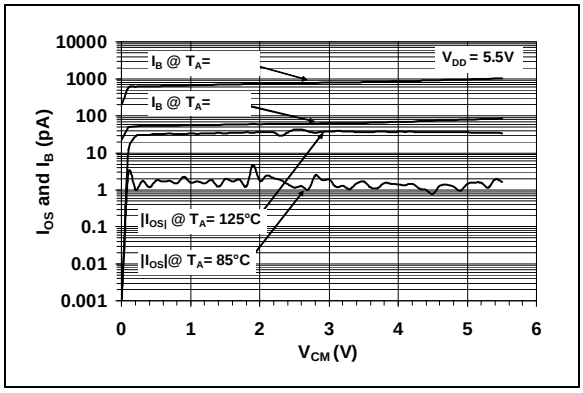


FIGURE 2-39: *Input Offset Current and Input Bias Current vs. Common-mode Input Voltage vs. Temperature.*

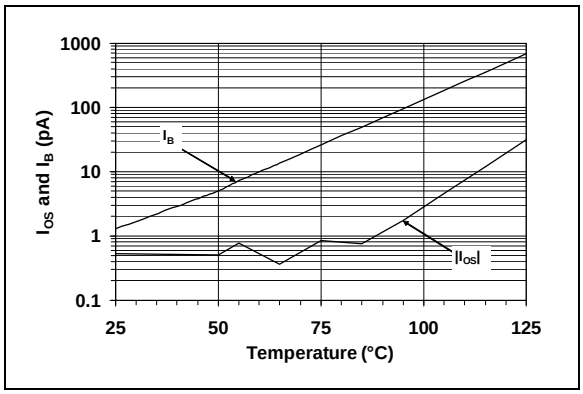


FIGURE 2-38: *Input Offset Current and Input Bias Current vs. Temperature.*

NOTES:

3.0 PIN DESCRIPTIONS

Descriptions of the pins are listed in Table 3-1.

TABLE 3-1: PIN FUNCTION TABLE

MCP6561	MCP6561R	MCP6561U	MCP6562	MCP6564	Symbol	Description
SC70-5, SOT-23-5	SOT-23-5	SOT-23-5	MSOP, SOIC	SOIC, TSSOP		
1	1	4	1	1	OUT, OUTA	Digital Output (comparator A)
4	4	3	2	2	$V_{IN}-$, $V_{INA}-$	Inverting Input (comparator A)
3	3	1	3	3	$V_{IN}+$, $V_{INA}+$	Non-inverting Input (comparator A)
5	2	5	8	4	V_{DD}	Positive Power Supply
—	—	—	5	5	$V_{INB}+$	Non-inverting Input (comparator B)
—	—	—	6	6	$V_{INB}-$	Inverting Input (comparator B)
—	—	—	7	7	OUTB	Digital Output (comparator B)
—	—	—	—	8	OUTC	Digital Output (comparator C)
—	—	—	—	9	$V_{INC}-$	Inverting Input (comparator C)
—	—	—	—	10	$V_{INC}+$	Non-inverting Input (comparator C)
2	5	2	4	11	V_{SS}	Negative Power Supply
—	—	—	—	12	$V_{IND}+$	Non-inverting Input (comparator D)
—	—	—	—	13	$V_{IND}-$	Inverting Input (comparator D)
—	—	—	—	14	OUTD	Digital Output (comparator D)

3.1 Analog Inputs

The comparator non-inverting and inverting inputs are high-impedance CMOS inputs with low bias currents.

3.2 Digital Outputs

The comparator outputs are CMOS, push-pull digital outputs. They are designed to be compatible with CMOS and TTL logic and are capable of driving heavy DC or capacitive loads.

3.3 Power Supply (V_{SS} and V_{DD})

The positive power supply pin (V_{DD}) is 1.8V to 5.5V higher than the negative power supply pin (V_{SS}). For normal operation, the other pins are at voltages between V_{SS} and V_{DD}.

Typically, these parts are used in a single (positive) supply configuration. In this case, V_{SS} is connected to ground and V_{DD} is connected to the supply. V_{DD} will need a local bypass capacitor (typically 0.01 µF to 0.1 µF) within 2 mm of the V_{DD} pin. These can share a bulk capacitor with nearby analog parts (within 100 mm), but it is not required.

NOTES:

4.0 APPLICATIONS INFORMATION

The MCP6561/1R/1U/2/4 family of push-pull output comparators are fabricated on Microchip's state-of-the-art CMOS process. They are suitable for a wide range of high speed applications requiring low power consumption.

4.1 Comparator Inputs

4.1.1 NORMAL OPERATION

The input stage of this family of devices uses three differential input stages in parallel: one operates at low-input voltages, one at high-input voltages, and one at mid-input voltage. With this topology, the input voltage range is 0.3V above V_{DD} and 0.3V below V_{SS}, while providing low offset voltage through out the Common-mode range. The input offset voltage is measured at both V_{SS} - 0.3V and V_{DD} + 0.3V to ensure proper operation.

The MCP6561/1R/1U/2/4 family has internally-set hysteresis V_{HYST} that is small enough to maintain input offset accuracy and large enough to eliminate output chattering caused by the comparator's own input noise voltage E_{NI}. Figure 4-1 depicts this behavior. Input offset voltage (V_{OS}) is the center (average) of the (input-referred) low-high and high-low trip points. Input hysteresis voltage (V_{HYST}) is the difference between the same trip points.

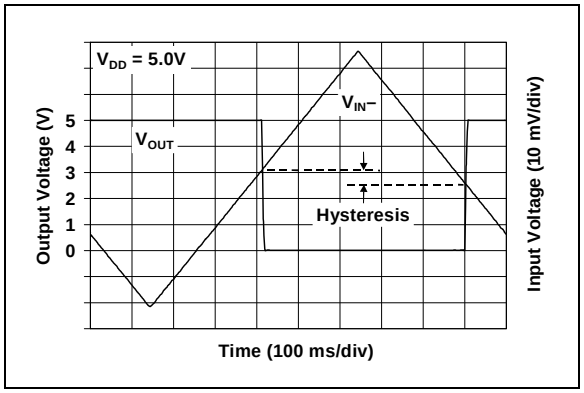


FIGURE 4-1: *The MCP6561/1R/1U/2/4 Comparators' Internal Hysteresis Eliminates Output Chatter Caused by Input Noise Voltage.*

4.1.2 INPUT VOLTAGE AND CURRENT LIMITS

The ESD protection on the inputs can be depicted as shown in Figure 4-2. This structure was chosen to protect the input transistors, and to minimize input bias current (I_B). The input ESD diodes clamp the inputs when they try to go more than one diode drop below V_{SS}. They also clamp any voltages that go too far above V_{DD}; their breakdown voltage is high enough to allow normal operation, and low enough to bypass ESD events within the specified limits.

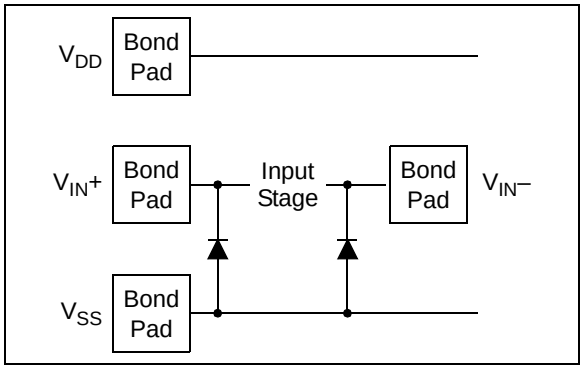


FIGURE 4-2: *Simplified Analog Input ESD Structures.*

In order to prevent damage and/or improper operation of these amplifiers, the circuits they are in must limit the currents (and voltages) at the V_{IN}+ and V_{IN}– pins (see Maximum Ratings † at the beginning of **Section 1.0 "Electrical Characteristics"**). Figure 4-3 shows the recommended approach to protecting these inputs. The internal ESD diodes prevent the input pins (V_{IN}+ and V_{IN}–) from going too far below ground, and the resistors R_1 and R_2 limit the possible current drawn out of the input pin. Diodes D_1 and D_2 prevent the input pin (V_{IN}+ and V_{IN}–) from going too far above V_{DD}. When implemented as shown, resistors R_1 and R_2 also limit the current through D_1 and D_2.

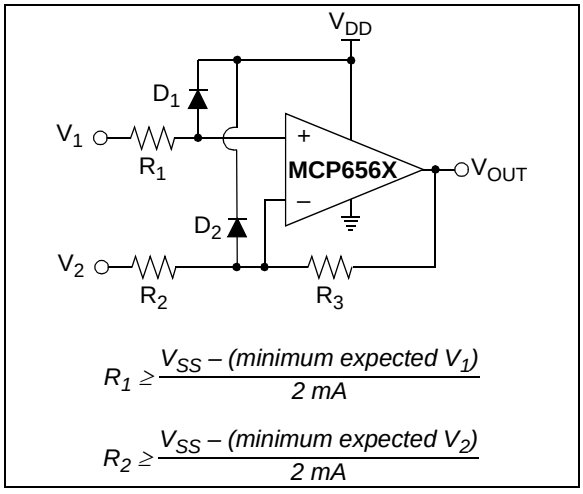


FIGURE 4-3: *Protecting the Analog Inputs.*

It is also possible to connect the diodes to the left of the resistors R_1 and R_2. In this case, the currents through the diodes D_1 and D_2 need to be limited by some other mechanism. The resistor then serves as in-rush current limiter; the DC current into the input pins (V_{IN}+ and V_{IN}–) should be very small.

A significant amount of current can flow out of the inputs when the Common-mode voltage (V_{CM}) is below ground (V_{SS}); see Figure 2-32. Applications that are high impedance may need to limit the usable voltage range.

4.1.3 PHASE REVERSAL

The MCP6561/1R/1U/2/4 comparator family uses CMOS transistors at the input. They are designed to prevent phase inversion when the input pins exceed the supply voltages. Figure 2-3 shows an input voltage exceeding both supplies with no resulting phase inversion.

4.2 Push-Pull Output

The push-pull output is designed to be compatible with CMOS and TTL logic, while the output transistors are configured to give rail-to-rail output performance. They are driven with circuitry that minimizes any switching current (shoot-through current from supply-to-supply) when the output is transitioned from high-to-low, or from low-to-high (see Figure 2-15 and Figure 2-18 for more information).

4.3 Externally Set Hysteresis

Greater flexibility in selecting hysteresis (or input trip points) is achieved by using external resistors. Hysteresis reduces output chattering when one input is slowly moving past the other. It also helps in systems where it is best not to cycle between high and low states too frequently (e.g., air conditioner thermostatic control). Output chatter also increases the dynamic supply current.

4.3.1 NON-INVERTING CIRCUIT

Figure 4-4 shows a non-inverting circuit for single-supply applications using just two resistors. The resulting hysteresis diagram is shown in Figure 4-5.

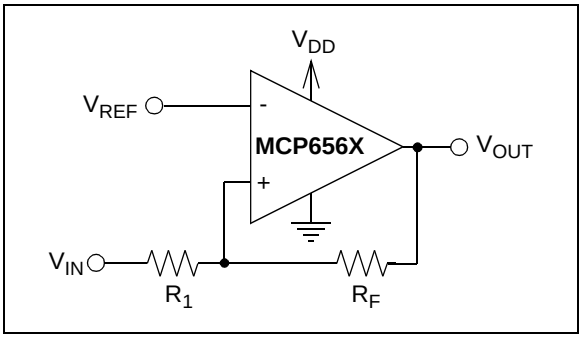


FIGURE 4-4: *Non-inverting Circuit with Hysteresis for Single-Supply.*

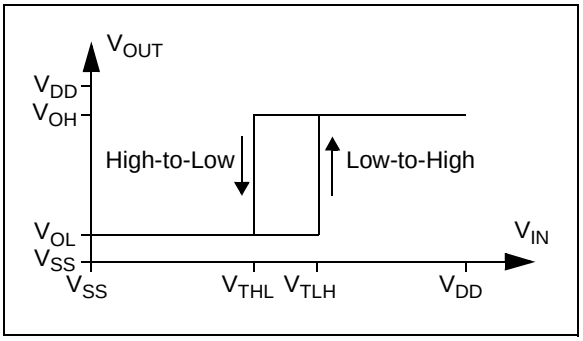


FIGURE 4-5: *Hysteresis Diagram for the Non-inverting Circuit.*

The trip points for Figure 4-4 and Figure 4-5 are:

EQUATION 4-1:

$$V_{TLH} = V_{REF}\left(1+\frac{R_1}{R_F}\right) - V_{OL}\left(\frac{R_1}{R_F}\right)$$

$$V_{THL} = V_{REF}\left(1+\frac{R_1}{R_F}\right) - V_{OH}\left(\frac{R_1}{R_F}\right)$$

Where:

V_{TLH} = trip voltage from low-to-high

V_{THL} = trip voltage from high-to-low

4.3.2 INVERTING CIRCUIT

Figure 4-6 shows an inverting circuit for single-supply using three resistors. The resulting hysteresis diagram is shown in Figure 4-7.

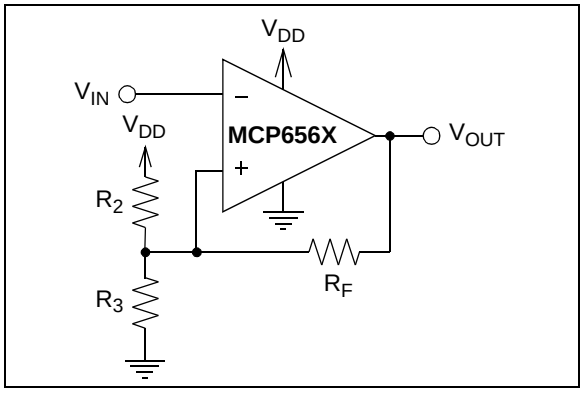


FIGURE 4-6: *Inverting Circuit With Hysteresis.*

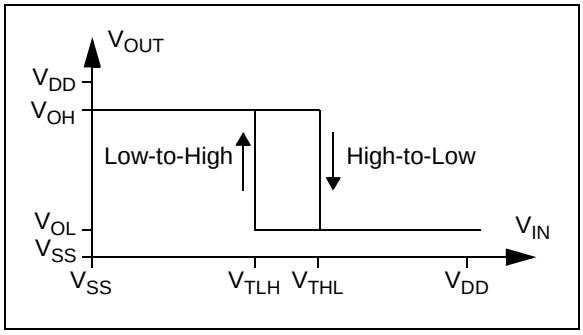


FIGURE 4-7: *Hysteresis Diagram for the Inverting Circuit.*

In order to determine the trip voltages (V_{THL} and V_{TLH}) for the circuit shown in Figure 4-6, R_2 and R_3 can be simplified to the Thevenin equivalent circuit with respect to V_{DD}, as shown in Figure 4-8.

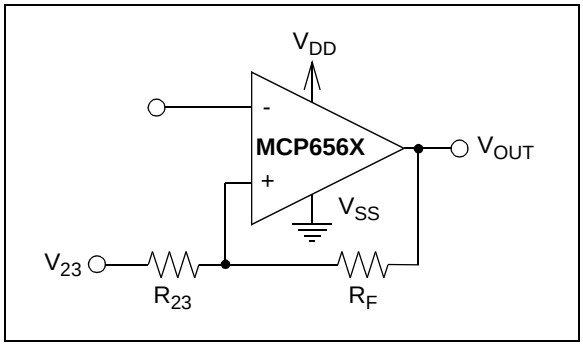


FIGURE 4-8: *Thevenin Equivalent Circuit.*

Where:

$$R_{23} = \frac{R_2 R_3}{R_2 + R_3}$$

$$V_{23} = \frac{R_3}{R_2 + R_3} \times V_{DD}$$

Using this simplified circuit, the trip voltage can be calculated using the following equation:

EQUATION 4-2:

$$V_{THL} = V_{OH}\left(\frac{R_{23}}{R_{23} + R_F}\right) + V_{23}\left(\frac{R_F}{R_{23} + R_F}\right)$$

$$V_{TLH} = V_{OL}\left(\frac{R_{23}}{R_{23} + R_F}\right) + V_{23}\left(\frac{R_F}{R_{23} + R_F}\right)$$

Where:

V_{TLH} = trip voltage from low-to-high

V_{THL} = trip voltage from high-to-low

Figure 2-20, and Figure 2-23 can be used to determine typical values for V_{OH} and V_{OL}.

4.4 Bypass Capacitors

With this family of comparators, the power supply pin (V_{DD} for single supply) should have a local bypass capacitor (i.e., 0.01 µF to 0.1 µF) within 2 mm for good edge rate performance.

4.5 Capacitive Loads

Reasonable capacitive loads (e.g., logic gates) have little impact on propagation delay (see Figure 2-31). The supply current increases with increasing toggle frequency (Figure 2-19), especially with higher capacitive loads. The output slew rate and propagation delay performance will be reduced with higher capacitive loads.

4.6 PCB Surface Leakage

In applications where low input bias current is critical, PCB (Printed Circuit Board) surface leakage effects need to be considered. Surface leakage is caused by humidity, dust or other contamination on the board. Under low humidity conditions, a typical resistance between nearby traces is $10^{12}\Omega$. A 5V difference would cause 5 pA of current to flow. This is greater than the MCP6561/1R/1U/2/4 family's bias current at +25°C (1 pA, typical).

The easiest way to reduce surface leakage is to use a guard ring around sensitive pins (or traces). The guard ring is biased at the same voltage as the sensitive pin. An example of this type of layout is shown in Figure 4-9.

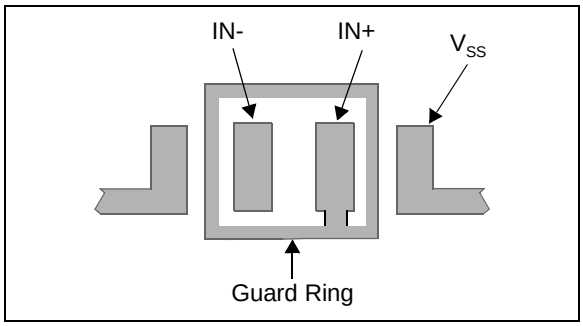


FIGURE 4-9: *Example Guard Ring Layout for Inverting Circuit.*

1. Inverting Configuration (Figures 4-6 and 4-9):
   a) Connect the guard ring to the non-inverting input pin (V_{IN}+). This biases the guard ring to the same reference voltage as the comparator (e.g., $V_{DD}/2$ or ground).
   b) Connect the inverting pin (V_{IN}-) to the input pad without touching the guard ring.
2. Non-inverting Configuration (Figure 4-4):
   a) Connect the non-inverting pin (V_{IN}+) to the input pad without touching the guard ring.
   b) Connect the guard ring to the inverting input pin (V_{IN}-).

4.7 PCB Layout Technique

When designing the PCB layout, it is critical to note that analog and digital signal traces are adequately separated to prevent signal coupling. If the comparator output trace is at close proximity to the input traces, then large output voltage changes from V_{SS} to V_{DD}, or visa versa, may couple to the inputs and cause the device output to oscillate. To prevent such oscillation, the output traces must be routed away from the input pins. The SC70-5 and SOT-23-5 are relatively immune because the output pin OUT (pin 1) is separated by the power pin V_{DD}/V_{SS} (pin 2) from the input pin +IN (as long as the analog and digital traces remain separated throughout the PCB). However, the pinouts for the dual and quad packages (SOIC, MSOP, TSSOP) have OUT and -IN pins (pin 1 and 2) close to each other. The recommended layout for these packages is shown in Figure 4-10.

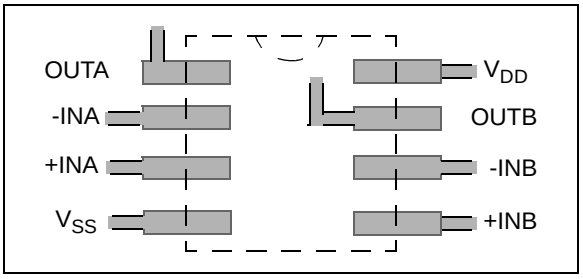


FIGURE 4-10: *Recommended Layout.*

4.8 Unused Comparators

An unused amplifier in a quad package (MCP6564) should be configured as shown in Figure 4-11. This circuit prevents the output from toggling and causing crosstalk. It uses the minimum number of components and draws minimal current (see Figure 2-15 and Figure 2-18).

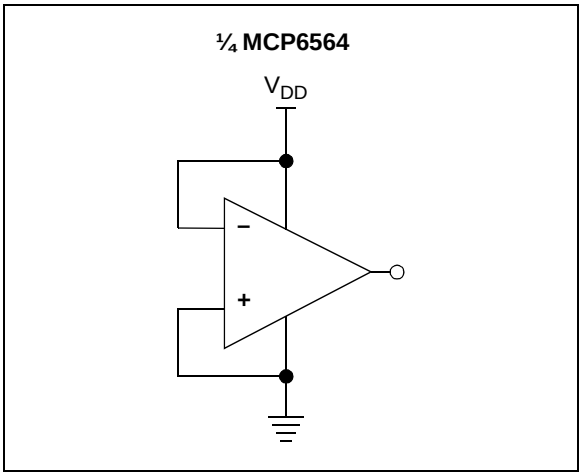


FIGURE 4-11: *Unused Comparators.*

4.9 Typical Applications

4.9.1 PRECISE COMPARATOR

Some applications require higher DC precision. An easy way to solve this problem is to use an amplifier (such as the MCP6291) to gain-up the input signal before it reaches the comparator. Figure 4-12 shows an example of this approach.

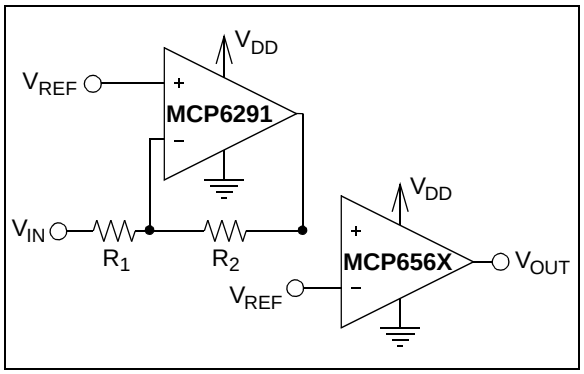


FIGURE 4-12: *Precise Inverting Comparator.*

4.9.2 WINDOWED COMPARATOR

Figure 4-13 shows one approach to designing a windowed comparator. The AND gate produces a logic '1' when the input voltage is between V_{RB} and V_{RT} (where $V_{RT} > V_{RB}$).

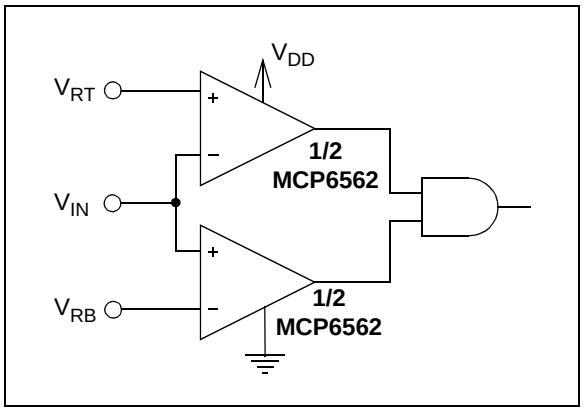


FIGURE 4-13: *Windowed Comparator.*

4.9.3 BISTABLE MULTIVIBRATOR

A simple bistable multivibrator design is shown in Figure 4-14. V_{REF} needs to be between the power supplies (V_{SS} = GND and V_{DD}) to achieve oscillation. The output duty cycle changes with V_{REF}.

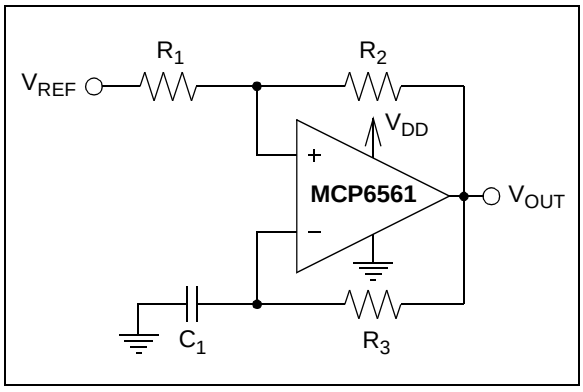


FIGURE 4-14: *Bistable Multivibrator.*

NOTES:

5.0 DESIGN AIDS

5.1 Microchip Advanced Part Selector (MAPS)

MAPS is a software tool that helps semiconductor professionals efficiently identify Microchip devices that fit a particular design requirement. Available at no cost from the Microchip web site at www.microchip.com/maps, the MAPS is an overall selection tool for Microchip's product portfolio that includes Analog, Memory, MCUs and DSCs. Using this tool you can define a filter to sort features for a parametric search of devices and export side-by-side technical comparison reports. Helpful links are also provided for data sheets, purchase, and sampling of Microchip parts.

5.2 Analog Demonstration and Evaluation Boards

Microchip offers a broad spectrum of Analog Demonstration and Evaluation Boards that are designed to help you achieve faster time to market. For a complete listing of these boards and their corresponding user's guides and technical information, visit the Microchip web site at www.microchip.com/analogtools. Three of our boards that are especially useful are:

- 8-Pin SOIC/MSOP/TSSOP/DIP Evaluation Board, P/N SOIC8EV
- 14-Pin SOIC/TSSOP/DIP Evaluation Board, P/N SOIC14EV
- 5/6-Pin SOT23 Evaluation Board, P/N VSUPEV2

5.3 Application Notes

The following Microchip Application Note is available on the Microchip web site at www.microchip.com and is recommended as a supplemental reference resource:

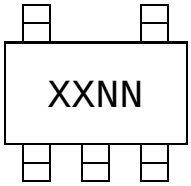
- **AN895,** *"Oscillator Circuits For RTD Temperature Sensors",* DS00895

NOTES:

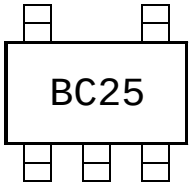
6.0 PACKAGING INFORMATION

6.1 Package Marking Information

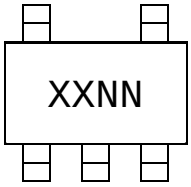
5-Lead SC-70 **(MCP6561)**



Example:



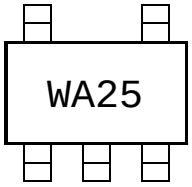
5-Lead SOT-23 **(MCP6561, MCP6561R, MCP6561U)**



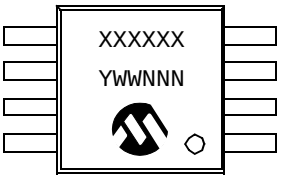
Device	Code
MCP6561T	WBNN
MCP6561RT	WANN
MCP6561UT	WKNN

Note: Applies to 5-Lead SOT-23.

Example:

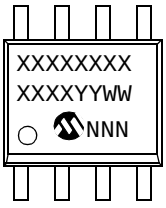


8-Lead MSOP **(MCP6562)**

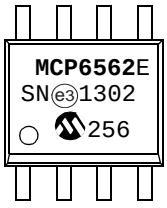


Example:

8-Lead SOIC (150 mil) **(MCP6562)**



Example:

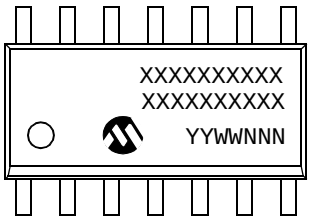


Legend:	XX...X	Customer-specific information
	Y	Year code (last digit of calendar year)
	YY	Year code (last 2 digits of calendar year)
	WW	Week code (week of January 1 is week ‘01’)
	NNN	Alphanumeric traceability code
	(e3)	Pb-free JEDEC designator for Matte Tin (Sn)
	*	This package is Pb-free. The Pb-free JEDEC designator ((e3)) can be found on the outer packaging for this package.

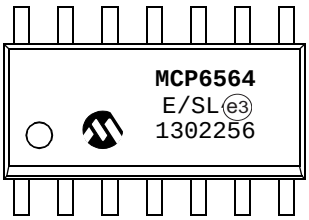
Note: In the event the full Microchip part number cannot be marked on one line, it will be carried over to the next line, thus limiting the number of available characters for customer-specific information.

Package Marking Information (Continued)

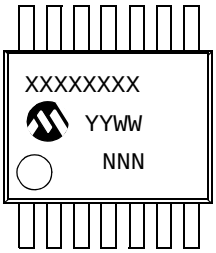
14-Lead SOIC (150 mil) **(MCP6564)**



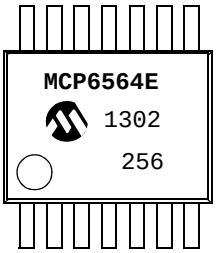
Example:



14-Lead TSSOP **(MCP6564)**

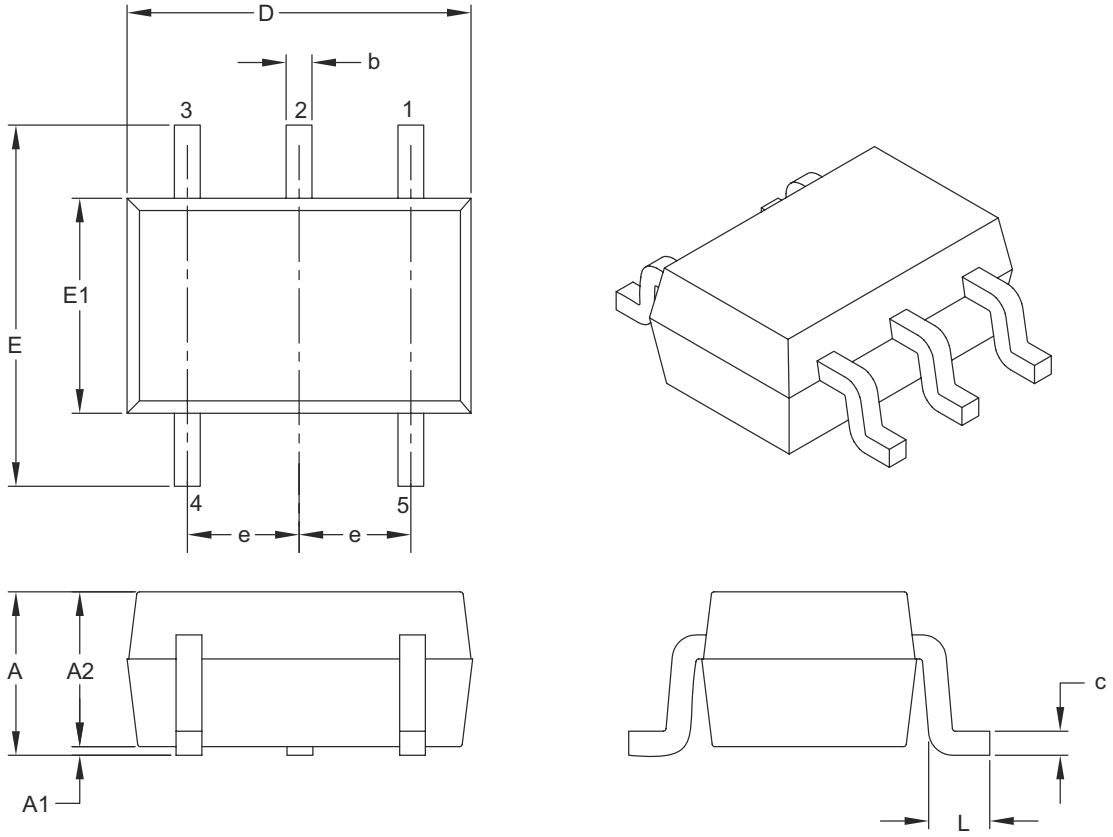


Example:



5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	–	1.10
Molded Package Thickness	A2	0.80	–	1.00
Standoff	A1	0.00	–	0.10
Overall Width	E	1.80	2.10	2.40
Molded Package Width	E1	1.15	1.25	1.35
Overall Length	D	1.80	2.00	2.25
Foot Length	L	0.10	0.20	0.46
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.15	–	0.40

Notes:

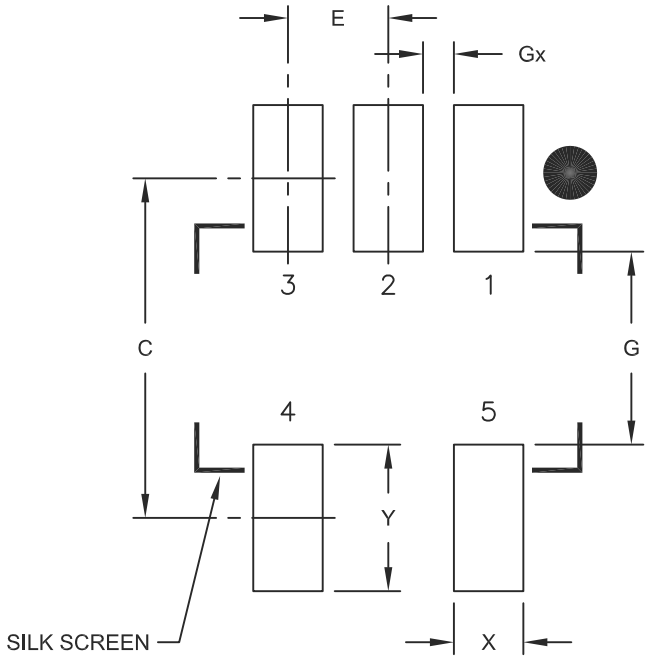
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-061B

5-Lead Plastic Small Outline Transistor (LT) [SC70]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		2.20	
Contact Pad Width	X			0.45
Contact Pad Length	Y			0.95
Distance Between Pads	G	1.25		
Distance Between Pads	Gx	0.20		

Notes:

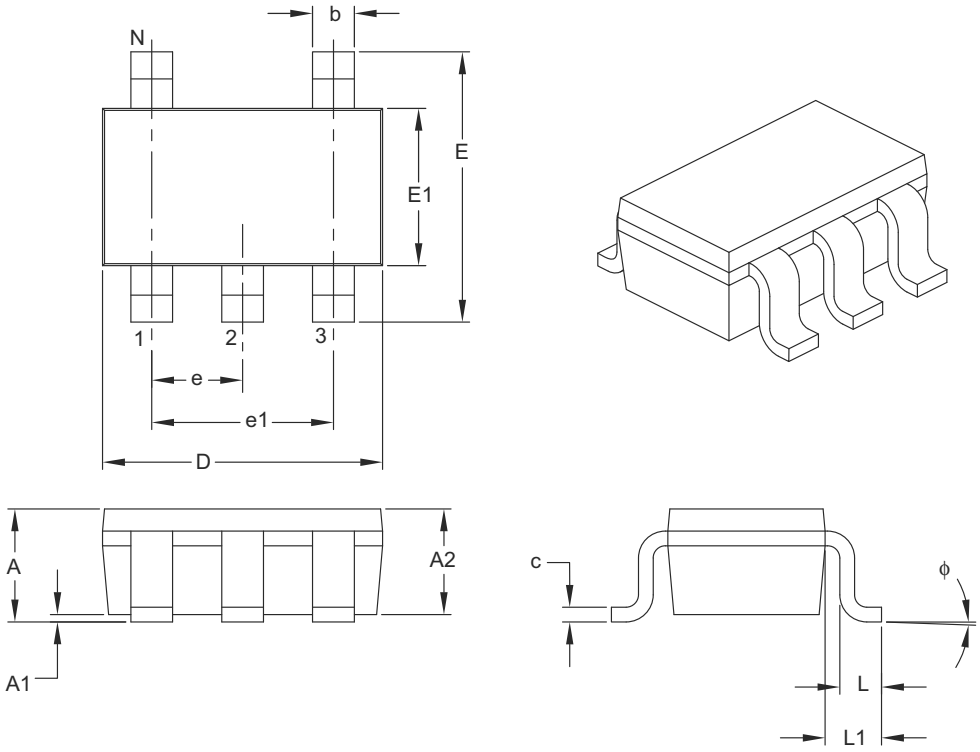
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2061A

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		5	
Lead Pitch	e		0.95 BSC	
Outside Lead Pitch	e1		1.90 BSC	
Overall Height	A	0.90	–	1.45
Molded Package Thickness	A2	0.89	–	1.30
Standoff	A1	0.00	–	0.15
Overall Width	E	2.20	–	3.20
Molded Package Width	E1	1.30	–	1.80
Overall Length	D	2.70	–	3.10
Foot Length	L	0.10	–	0.60
Footprint	L1	0.35	–	0.80
Foot Angle	ϕ	0°	–	30°
Lead Thickness	c	0.08	–	0.26
Lead Width	b	0.20	–	0.51

Notes:

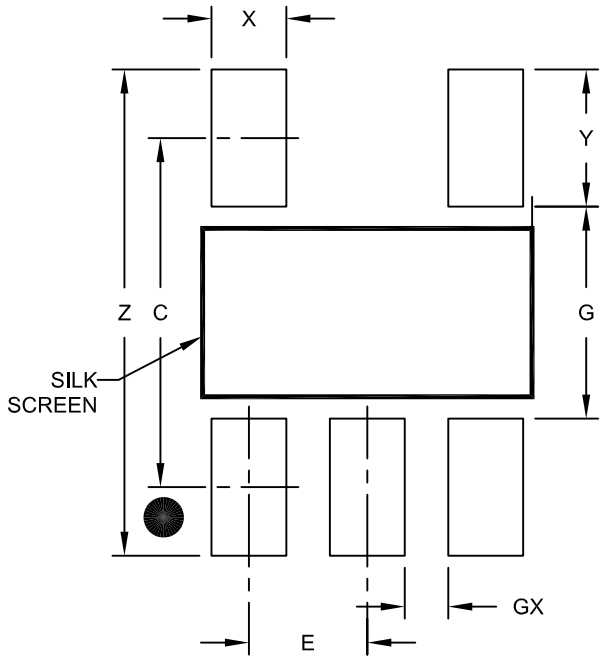
1. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.127 mm per side.
2. Dimensioning and tolerancing per ASME Y14.5M.

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing C04-091B

5-Lead Plastic Small Outline Transistor (OT) [SOT-23]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.95 BSC	
Contact Pad Spacing	C		2.80	
Contact Pad Width (X5)	X			0.60
Contact Pad Length (X5)	Y			1.10
Distance Between Pads	G	1.70		
Distance Between Pads	GX	0.35		
Overall Width	Z			3.90

Notes:

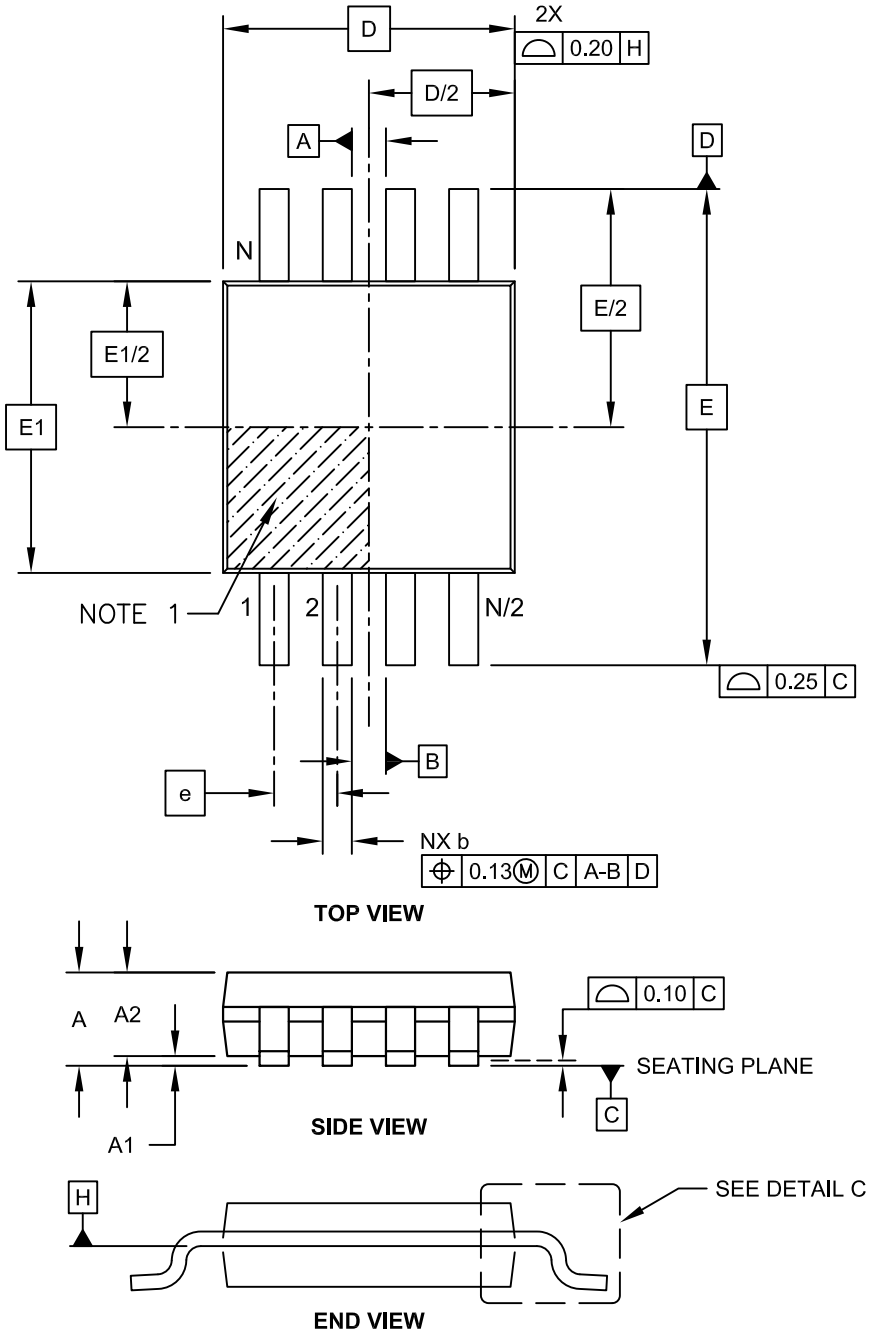
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2091A

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

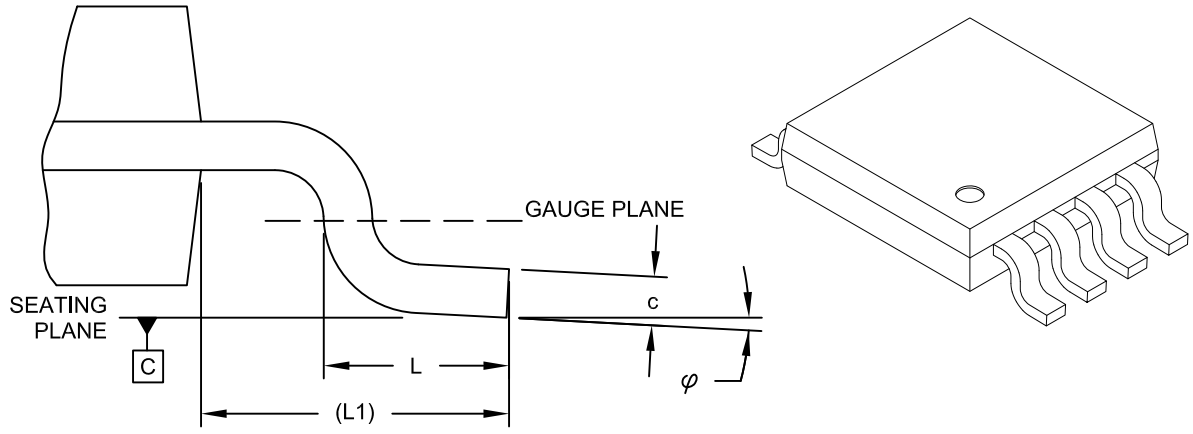
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Microchip Technology Drawing C04-111C Sheet 1 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



DETAIL C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.10
Molded Package Thickness	A2	0.75	0.85	0.95
Standoff	A1	0.00	-	0.15
Overall Width	E		4.90 BSC	
Molded Package Width	E1		3.00 BSC	
Overall Length	D		3.00 BSC	
Foot Length	L	0.40	0.60	0.80
Footprint	L1		0.95 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.08	-	0.23
Lead Width	b	0.22	-	0.40

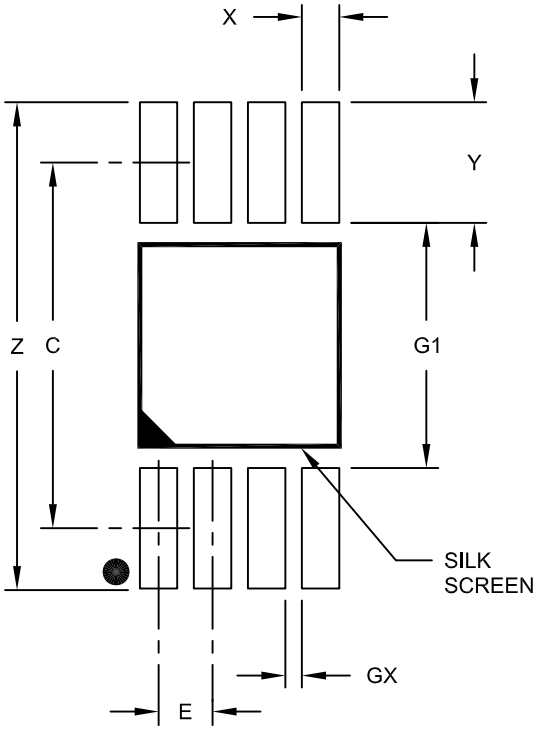
Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M.
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.
   REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing C04-111C Sheet 2 of 2

8-Lead Plastic Micro Small Outline Package (MS) [MSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		0.65 BSC	
Contact Pad Spacing	C		4.40	
Overall Width	Z			5.85
Contact Pad Width (X8)	X1			0.45
Contact Pad Length (X8)	Y1			1.45
Distance Between Pads	G1	2.95		
Distance Between Pads	GX	0.20		

Notes:

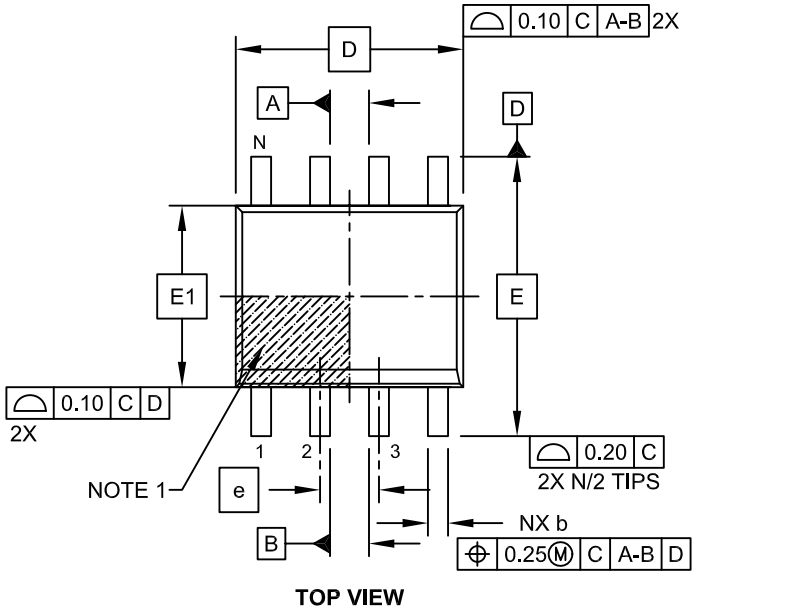
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

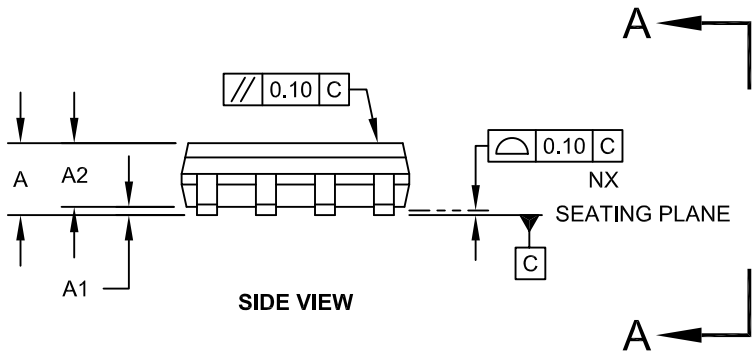
Microchip Technology Drawing No. C04-2111A

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

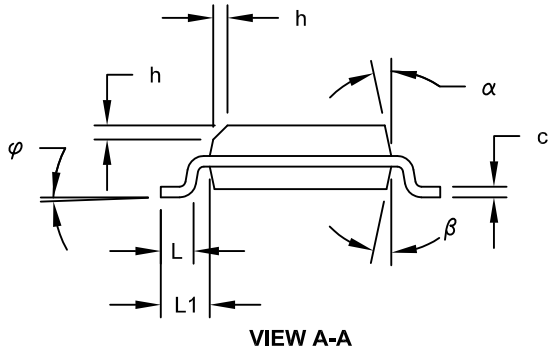
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

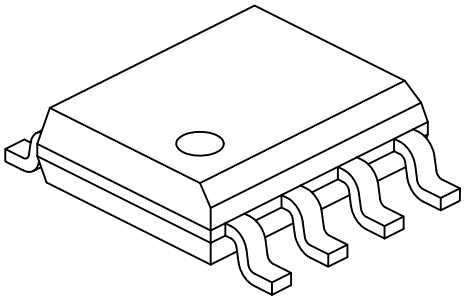


VIEW A-A

Microchip Technology Drawing No. C04-057C Sheet 1 of 2

8-Lead Plastic Small Outline (SN) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		8	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		4.90 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.17	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

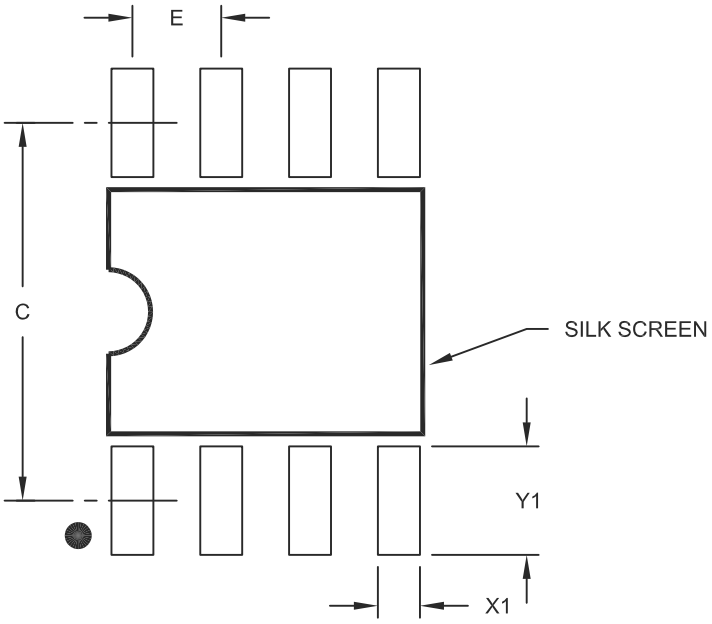
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-057C Sheet 2 of 2

8-Lead Plastic Small Outline (SN) – Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width (X8)	X1			0.60
Contact Pad Length (X8)	Y1			1.55

Notes:

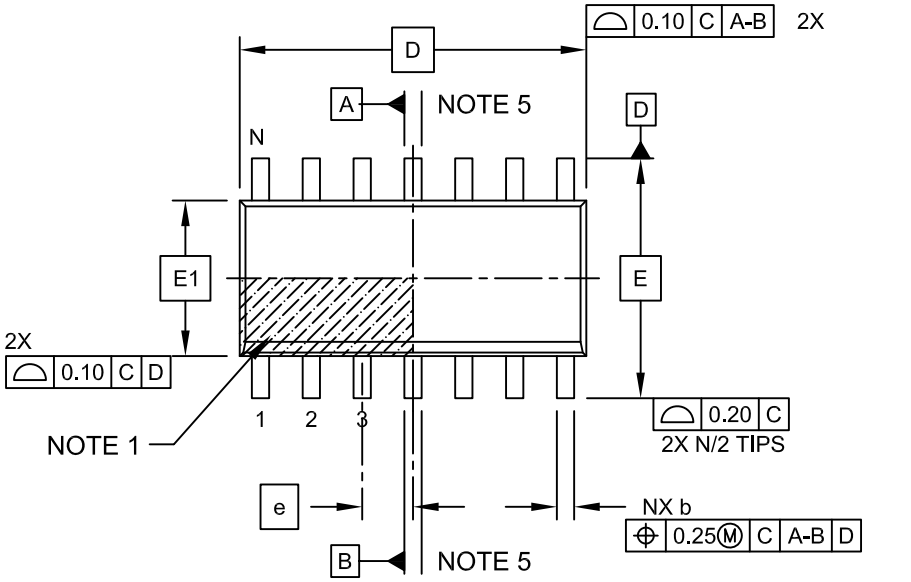
1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

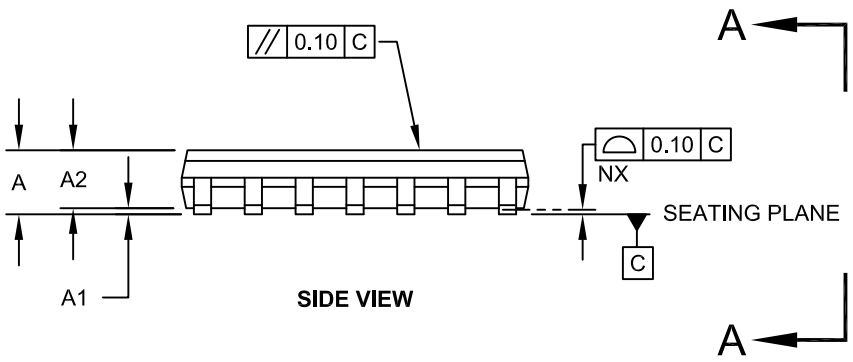
Microchip Technology Drawing No. C04-2057A

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

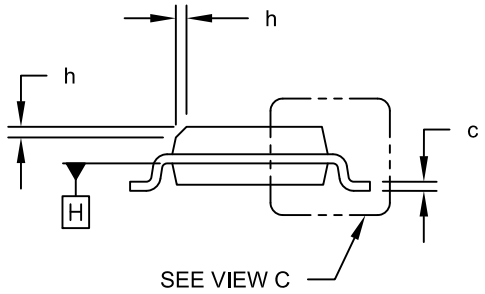
Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



TOP VIEW



SIDE VIEW

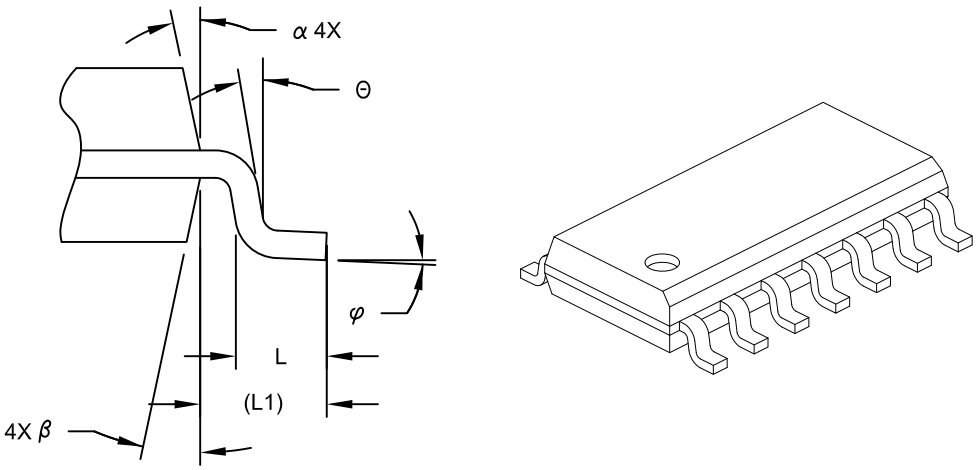


VIEW A-A

Microchip Technology Drawing No. C04-065C Sheet 1 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



VIEW C

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		1.27 BSC	
Overall Height	A	-	-	1.75
Molded Package Thickness	A2	1.25	-	-
Standoff §	A1	0.10	-	0.25
Overall Width	E		6.00 BSC	
Molded Package Width	E1		3.90 BSC	
Overall Length	D		8.65 BSC	
Chamfer (Optional)	h	0.25	-	0.50
Foot Length	L	0.40	-	1.27
Footprint	L1		1.04 REF	
Lead Angle	Θ	0°	-	-
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.10	-	0.25
Lead Width	b	0.31	-	0.51
Mold Draft Angle Top	α	5°	-	15°
Mold Draft Angle Bottom	β	5°	-	15°

Notes:

1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. § Significant Characteristic
3. Dimension D does not include mold flash, protrusions or gate burrs, which shall not exceed 0.15 mm per end. Dimension E1 does not include interlead flash or protrusion, which shall not exceed 0.25 mm per side.
4. Dimensioning and tolerancing per ASME Y14.5M

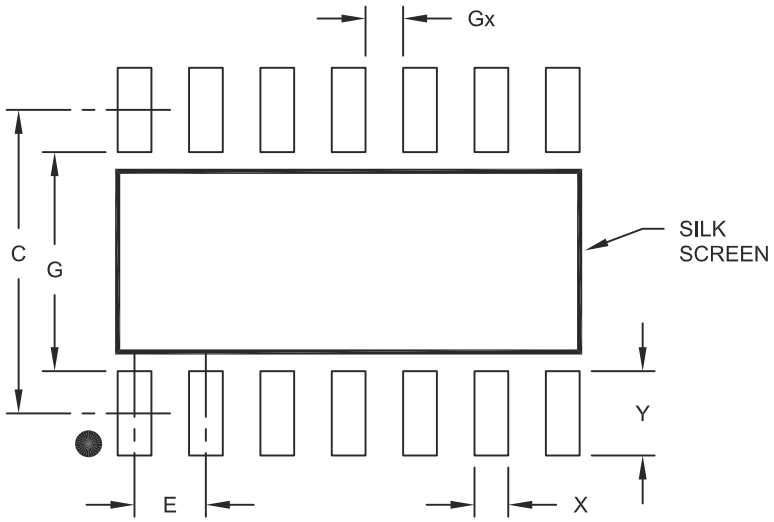
   BSC: Basic Dimension. Theoretically exact value shown without tolerances.

   REF: Reference Dimension, usually without tolerance, for information purposes only.
5. Datums A & B to be determined at Datum H.

Microchip Technology Drawing No. C04-065C Sheet 2 of 2

14-Lead Plastic Small Outline (SL) - Narrow, 3.90 mm Body [SOIC]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E		1.27 BSC	
Contact Pad Spacing	C		5.40	
Contact Pad Width	X			0.60
Contact Pad Length	Y			1.50
Distance Between Pads	Gx	0.67		
Distance Between Pads	G	3.90		

Notes:

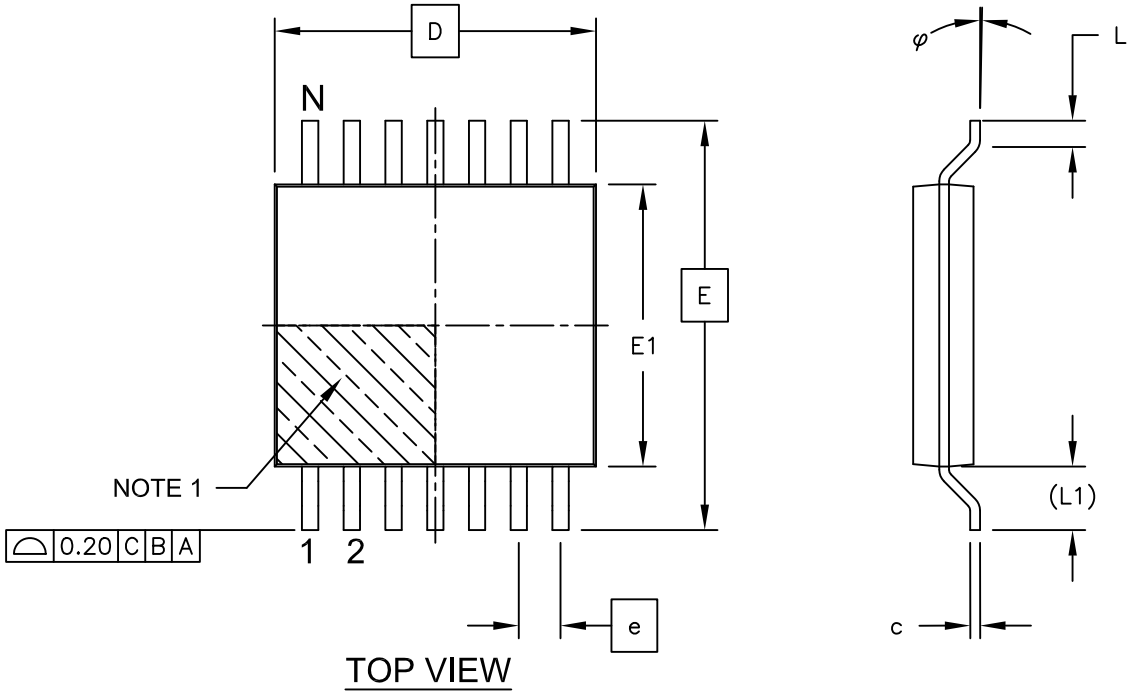
1. Dimensioning and tolerancing per ASME Y14.5M

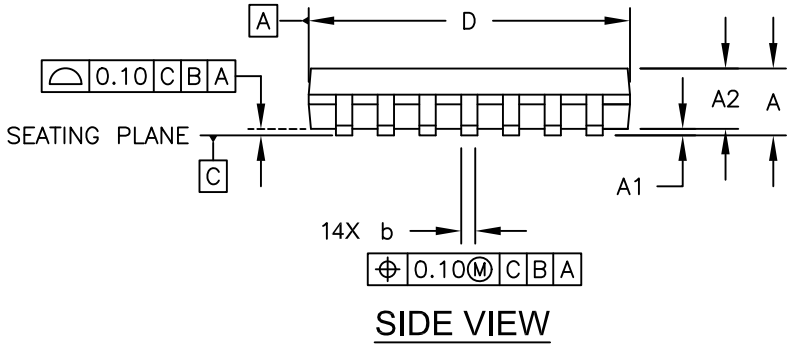
BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2065A

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging

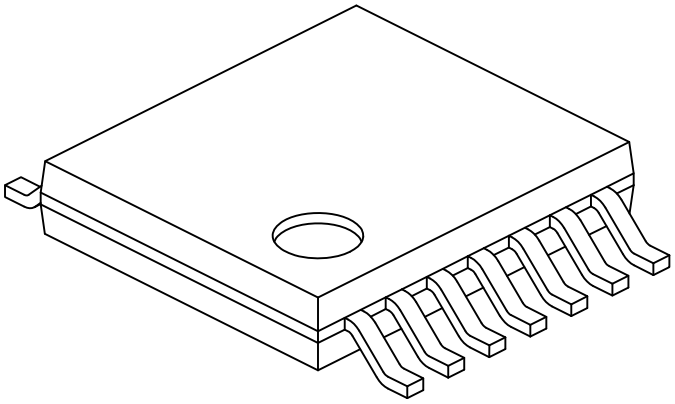




Microchip Technology Drawing C04-087C Sheet 1 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Number of Pins	N		14	
Pitch	e		0.65 BSC	
Overall Height	A	-	-	1.20
Molded Package Thickness	A2	0.80	1.00	1.05
Standoff	A1	0.05	-	0.15
Overall Width	E		6.40 BSC	
Molded Package Width	E1	4.30	4.40	4.50
Molded Package Length	D	4.90	5.00	5.10
Foot Length	L	0.45	0.60	0.75
Footprint	(L1)		1.00 REF	
Foot Angle	φ	0°	-	8°
Lead Thickness	c	0.09	-	0.20
Lead Width	b	0.19	-	0.30

Notes:

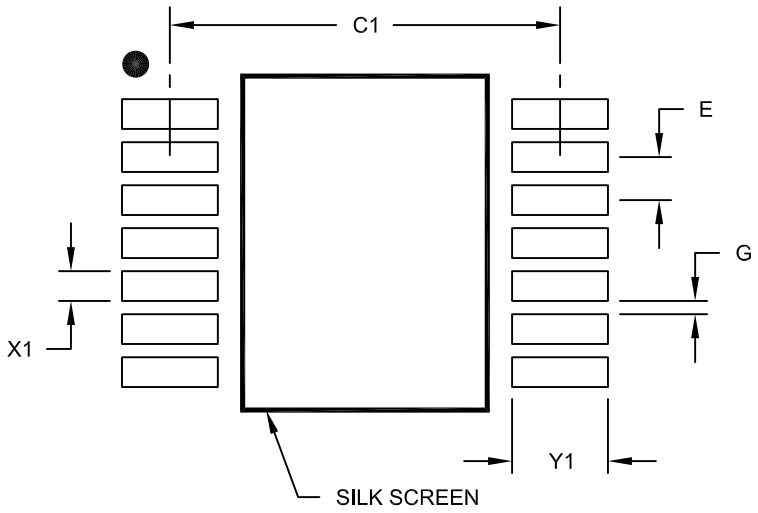
1. Pin 1 visual index feature may vary, but must be located within the hatched area.
2. Dimensions D and E1 do not include mold flash or protrusions. Mold flash or protrusions shall not exceed 0.15mm per side.
3. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.
REF: Reference Dimension, usually without tolerance, for information purposes only.

Microchip Technology Drawing No. C04-087C Sheet 2 of 2

14-Lead Plastic Thin Shrink Small Outline (ST) - 4.4 mm Body [TSSOP]

Note: For the most current package drawings, please see the Microchip Packaging Specification located at http://www.microchip.com/packaging



RECOMMENDED LAND PATTERN

Units		MILLIMETERS		
Dimension Limits		MIN	NOM	MAX
Contact Pitch	E	0.65 BSC		
Contact Pad Spacing	C1		5.90	
Contact Pad Width (X28)	X1			0.45
Contact Pad Length (X28)	Y1			1.45
Distance Between Pads	G	0.20		

Notes:

1. Dimensioning and tolerancing per ASME Y14.5M

BSC: Basic Dimension. Theoretically exact value shown without tolerances.

Microchip Technology Drawing No. C04-2087A

APPENDIX A: REVISION HISTORY

Revision C (February 2013)

The following is the list of modifications:

1. Added the Analog Input (V_{IN}) parameter in **Section 1.0 "Electrical Characteristics"**.
2. Updated the package drawing section.

Revision B (August 2009)

The following is the list of modifications:

1. Added MCP6561U throughout the document.
2. Updated package drawing section.

Revision A (March 2009)

- Original Release of this Document.

NOTES:

PRODUCT IDENTIFICATION SYSTEM

To order or obtain information, e.g., on pricing or delivery, refer to the factory or the listed sales office.

PART NO.	–	X	/XX
Device		Temperature Range	Package

Device:	MCP6561T:	Single Comparator (Tape and Reel) (SC70, SOT-23)
	MCP6561RT:	Single Comparator (Tape and Reel) (SOT-23 only)
	MCP6561UT:	Single Comparator (Tape and Reel) (SOT-23 only)
	MCP6562:	Dual Comparator
	MCP6562T:	Dual Comparator (Tape and Reel)
	MCP6564:	Quad Comparator
	MCP6564T:	Quad Comparator(Tape and Reel)
Temperature Range:	E =	-40°C to +125°C
Package:	LT =	Plastic Small Outline Transistor (SC70), 5-lead
	OT =	Plastic Small Outline Transistor, 5-lead
	MS =	Plastic Micro Small Outline Transistor, 8-lead
	SN =	Plastic Small Outline Transistor, 8-lead
	ST =	Plastic Thin Shrink Small Outline Transistor, 14-lead
	SL =	Plastic Small Outline Transistor, 14-lead

Examples:

a)	MCP6561T-E/LT:	Tape and Reel, Extended Temperature, 5LD SC70 package.
b)	MCP6561T-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package.
a)	MCP6561RT-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package.
a)	MCP6561UT-E/OT:	Tape and Reel, Extended Temperature, 5LD SOT-23 package.
a)	MCP6562-E/MS:	Extended Temperature, 8LD MSOP package.
b)	MCP6562-E/SN:	Extended Temperature, 8LD SOIC package.
a)	MCP6564T-E/SL:	Tape and Reel, Extended Temperature, 14LD SOIC package.
b)	MCP6564T-E/ST:	Tape and Reel, Extended Temperature, 14LD TSSOP package.

NOTES:

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